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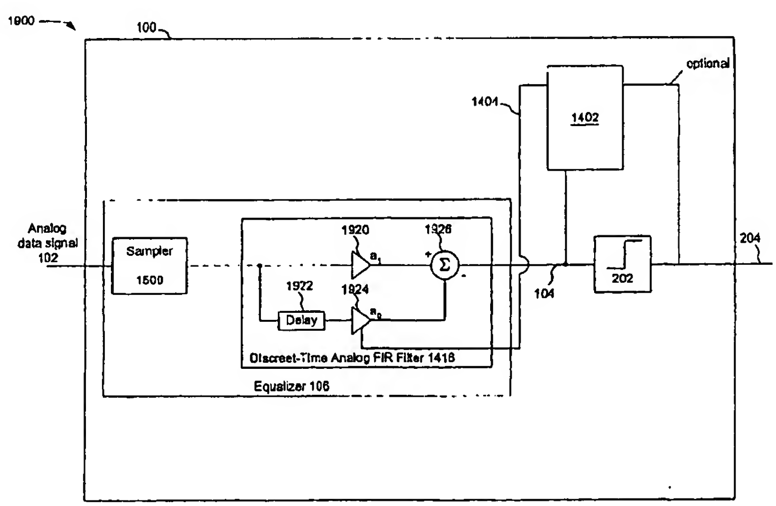
(54) Title: METHODS AND SYSTEMS FOR ADAPTIVE RECEIVER EQUALIZATION



(57) Abstract: Methods and systems for minimizing distortions in an analog data signal include equalizing the analog data signal at a receive end. In an embodiment, the invention adapts equalization parameters to a signal path associated with the analog data signal. Adaptive control logic is implemented with analog and/or digital components. In an embodiment, the invention equalizes a discreet-time analog representation of an analog data signal. In an embodiment, the invention digitally controls equalization parameters. In an embodiment, a resultant equalized analog data signal is digitized. In an example implementation, an analog data signal is sampled, a quality of the samples is measured, and one or more equalization parameters are adjusted with digital controls as needed to minimize distortion of the samples. The equalized samples are then digitized. The present invention is suitable for lower rate analog data signals and multi-gigabit data rate analog signals.

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METHODS AND SYSTEMS FOR ADAPTIVE RECEIVER EQUALIZATION

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention is directed to analog signal receivers and, more particularly, to methods and systems for equalizing (e.g., minimizing distortions within) analog data signals.

Background Art

Conventional signal propagation mediums, such as conventional backplane material (e.g., FR4) and conventional wires (e.g., IEEE 1394 "firewire)," are generally suitable for lower data rate signals, up to about 622 megabits per second. At higher frequencies, however, data signals are increasingly subject to frequency band-limiting distortions such as inter-symbol interference.

Inter-symbol interference results, in part, from unsettled response times following signal state changes. In other words, when a first state change does not settle before a second state change, the state changes can begin to overlap and can become more difficult to distinguish from one another.

A conventional approach compensates for inter-symbol interference with pre-emphasis, which boosts signal amplitudes prior to transmission. Pre-emphasis techniques typically require prior knowledge of signal paths. When an integrated circuit ("IC") is intended to be used in multiple systems, the IC needs to be pre-programed for various system characterizations. This is costly, time-consuming, and inefficient. Pre-emphasis also typically causes electromagnetic interference problems such as impedance mismatching and other reflective problems.

What is needed is a method and system for minimizing frequency band-limiting distortions, such as inter-symbol interference, in analog data signals. What is also needed is a method and system for adaptively minimizing frequency

band-limiting distortions, such as inter-symbol interference, in analog data signals.

BRIEF SUMMARY OF THE INVENTION

The present invention is directed to methods and systems for minimizing distortions in an analog data signal at a receive end.

In an embodiment, the invention adapts equalization parameters to a signal path associated with the analog data signal. Adaptive control logic is implemented with analog and/or digital components.

In an embodiment, the invention equalizes a discreet-time analog representation of an analog data signal. In an embodiment, the invention equalizes a discreet-time analog representation of an analog data signal using digital controls.

In an embodiment, a resultant equalized analog data signal is digitized.

In an example implementation, an analog data signal is sampled, a quality of the samples is measured, and one or more equalization parameters are adjusted with digital controls as needed to minimize distortion of the samples. The equalized samples are then digitized.

The present invention is suitable for lower rate analog data signals and multi-gigabit data rate analog signals.

BRIEF DESCRIPTION OF THE DRAWINGS/FIGURES

FIG. 1 is a high level block diagram of an example analog data receiver 100 in accordance with an aspect of the present invention;

FIG. 2 is a block diagram of an example embodiment of the analog data receiver illustrated in FIG. 1;

FIG. 3 is a block diagram of an example serial-to-parallel analog data receiver in accordance with an aspect of the present invention;

FIG. 4 is a block diagram of an example transceiver in accordance with an aspect of the present invention;

FIG. 5 is a block diagram of a multi-channel implementation of a receiver, in accordance with an aspect of the present invention;

FIG. 6 is a block diagram of the example transceiver illustrated in FIG. 4;

FIG. 7 is an example dual-path receiver implementation of the analog data receiver illustrated in FIG. 1;

FIG. 8 is a block diagram of an example multi-path receiver implementation of the analog data receiver illustrated in FIG. 1;

FIG. 9 illustrates example clocking signals in accordance with an aspect of the present invention;

FIG. 10 is a block diagram of an example router in accordance with an aspect of the present invention;

FIG. 11A is an example eye diagram for a 3.125 gigabits per second analog data signal after propagation through thirty-six inches of conventional FR4 backplane material;.

FIG. 11B is an example eye diagram for a 3.125 gigabits per second analog data signal after propagation through twenty-five feet of IEEE 1394 "firewire;"

FIG. 12 illustrates an example non-return-to-zero ("NRZ") analog data signal;

FIG. 13A is an example eye diagram for a 3.125 gigabits per second analog data signal after propagation through thirty-six inches of conventional FR4 backplane material, after analog receive equalization is performed in accordance the present invention;

FIG. 13B is an example eye diagram for a 3.125 gigabits per second analog data signal after propagation through twenty-five feet of IEEE 1394 "firewire," after equalization is performed in accordance with the present invention;

FIG. 14A is a block diagram of an example implementation of the receiver illustrated in FIG. 1;

FIG. 14B is a block diagram of an example implementation of the receiver illustrated in FIG. 2;

FIG. 14C is a block diagram of an example implementation of the receiver illustrated in FIG. 1;

FIG. 14D is a block diagram of an example implementation of the receiver illustrated in FIG. 1;

FIG. 14E is a block diagram of an example implementation of the receiver illustrated in FIG. 1;

FIG. 14F illustrates example implementations of an analog finite impulse response filter illustrated in FIG. 14E;

FIG. 14G illustrates example implementations of an analog finite impulse response filter illustrated in FIG. 14E;

FIG. 14H is a block diagram of an example implementation of the receiver illustrated in FIG. 1;

FIG. 15 is a block diagram of an example discreet-time analog implementation of the present invention;

FIG. 16 is a block diagram of an example discreet-time analog dual path implementation of the present invention;

FIG. 17 is a block diagram of an example implementation of the receiver illustrated in FIG. 16;

FIG. 18 is a block diagram of an example implementation of the receiver illustrated in FIG. 16;

FIG. 19 is a block diagram of an example single-tap discreet-time analog implementation of the present invention;

FIG. 20 is a block diagram of an example implementation of a quality measuring and adaptive control module in accordance with an aspect of the present invention;

FIGS. 21A is a block diagram of an example implementation of a portion of the quality measuring and adaptive control module illustrated in FIG. 20;

FIGS. 21B is a block diagram of an example implementation of a portion of the quality measuring and adaptive control module illustrated in FIG. 20;

FIGS. 21C is a block diagram of an example implementation of a portion of the quality measuring and adaptive control module illustrated in FIG. 20;

FIGS. 21D is an example state diagram for a state machine illustrated in FIGS. 21B and 21C;

FIG. 22 is a block diagram of an example multi-path receiver, in accordance with an aspect of the present invention;

FIG. 23 is a block diagram of an example discreet-time analog multi-channel, multi-path receiver in accordance with an aspect of the present invention;

FIG. 24 is an example process flowchart for adaptively equalizing an analog information signal for a given signal path, in accordance with an aspect of the present invention;.

FIG. 25 is an example process flowchart for implementing the flowchart illustrated in FIG. 24;

FIG. 26 is an example process flowchart for implementing the flowchart illustrated in FIG. 24;

FIG. 27 is an example process flowchart for implementing the flowchart illustrated in FIG. 26;

FIG. 28 is an example process flowchart for adaptively equalizing time-staggered portions of an analog information signal for a given signal path, in accordance with an aspect of the present invention;

FIG. 29 is an example process flowchart for adaptively equalizing a plurality of time-staggered portions of multiple information signals for their respective signal paths, in accordance with an aspect of the present invention; and

FIG. 30 is an example process flowchart for adaptively equalizing a plurality of analog information signals for their respective signal paths, in accordance with an aspect of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

I. Introduction

Conventional backplane materials, such as FR4, and conventional wires such as IEEE 1494 "firewire," are suitable for lower data rates up to about 622 megabits per second. At higher data rates, however, data signals are increasingly subject to frequency band-limiting distortion, such as inter-symbol distortion, inter-channel interference, attenuation, cross-talk, etc.

FIG. 11A is an example eye diagram for a 3.125 gigabits per second analog data signal after propagation through thirty-six inches of conventional FR4 backplane material.

FIG. 11B is an example eye diagram for a 3.125 gigabits per second analog data signal after propagation through twenty-five feet of IEEE 1394 "firewire."

Signals corresponding to the eye diagrams as illustrated in FIGS. 11A and 11B are difficult to digitize because of the excessive inter-symbol distortion..

In accordance with the invention, inter-symbol distortion of an analog data signal is minimized through equalization of the received analog data signal. In other words, the present invention opens the eye of the received analog data signal.

Similarly, FIG. 12 is an example non-return-to-zero ("NRZ") analog data signal 1200. Inter-symbol distortion is evident in post transition amplitude 1204, which does not have time to reach zero, and post transition amplitude 1208, which does not have time to reach the steady state amplitude 1206.

In accordance with the present invention, analog receive equalization minimizes differences between amplitudes of the analog data signal 1200 just after transitions (e.g., 1202, 1204), and amplitudes of the analog data signal at steady state (e.g., 1206).

FIG. 13A is an example eye diagram for a 3.125 gigabits per second analog data signal after propagation through thirty-six inches of conventional FR4 backplane material, after analog receive equalization is performed in accordance with the present invention.

FIG. 13B is an example eye diagram for a 3.125 gigabits per second analog data signal after propagation through twenty-five feet of IEEE 1394 "firewire," after analog receiver equalization is performed in accordance with the present invention.

II. Example Environments

An analog data receiver in accordance with the present invention can be implemented in one or more of a variety of receiver environments. Various example receiver environments are illustrated and/or described herein in which the present invention can be implemented. The present invention is not, however, limited to the example environments illustrated and/or described herein. Based on the illustrations and description herein, one skilled in the relevant art(s) will understand that the present invention can be implemented in other environments and systems as well. Such other environments and systems are within the scope of the present invention.

FIG. 1 is a high level block diagram of an example analog data receiver 100, including an equalizer 106, in accordance with the present invention. The example analog data receiver 100 receives an analog data signal 102. The analog data signal 102 can include higher rate analog data signals, such as, without limitation, multi-gigabit (e.g. 3 GHz) analog data signals. The equalizer 106

equalizes the analog data signal 102 and outputs an equalized analog data signal 104.

In an embodiment, the equalizer 106 is adapts in real time to a signal path associated with the analog data signal 102, and/or to changing distortions. Alternatively, the equalizer 106 is implemented to provide a fixed amount of equalization.

In an embodiment, the equalizer 106 adapts to minimize inter-symbol distortion that arises from various transmission paths including, without limitation, various lengths of IEEE 1394 "firewire," FR4 backplane material, and other conventional and non-conventional sources of inter-symbol distortion. In an adaptive implementation, the equalizer 106 does not require prior knowledge of signal paths and thus can be utilized in a variety of conventional systems without substantial re-design of the existing systems.

In an embodiment, the equalizer 106 is implemented with one or more filters. Generally, filters designed for high data rate analog signals are expensive to implement. However, the present invention provides adaptive hybrid analog/digital high data rate filtering methods and systems that are uncomplicated and inexpensive to implement.

The equalizer 106 is suitable for non-return to zero ("NRZ") protocols as well as other protocols.

In an embodiment, the receiver 100 outputs the equalized analog data signal 104. Alternatively, or additionally, the receiver 100 converts the equalized analog data signal 104 to one or more digital signals which can include, without limitation, one or more serial digital data signals and/or one or more parallel digital data signals.

For example, FIG. 2 is a block diagram of an example embodiment of the analog data receiver 100 further including an optional quantizer 202, which over-samples the quantized analog data signal 104 to convert it to the one or more digital data signals 204. Based on the description herein, one skilled in the relevant art(s) will understand that the quantizer 202, and/or other digitizing

methods and/or systems, can be implemented as one or more of a variety of conventional quantizers.

The optional quantizer 202, and/or other digitizing methods and/or systems, can be utilized in a variety of receiver embodiments including, without limitation, receiver embodiments described and/or illustrated herein. However, the present invention can be implemented without digitizing the equalized analog signal 104.

In an embodiment, the equalizer 106 operates directly on the analog data signal 102. Alternatively, the equalizer 106 operates on discreet-time analog "slices" or "samples" of the analog data signal 102. Because each slice or sample is a substantially constant analog level, the optional equalizer 202 equalizes higher data rate signals as well as lower data rate signals. Methods and systems for discreet-time equalization of the analog data signal 102 are described below.

FIG. 3 is a block diagram of an example serial-to-parallel analog data receiver 300 implementation of the receiver 200, which outputs a parallel digital data signal 302. The serial-to-parallel analog data receiver 300 also receives a clock signal 304 and outputs a clock signal 306.

The present invention can be implemented within a variety of types of transceivers. FIG. 4 is a block diagram of an example transceiver 400 that includes the analog data receiver 100 and an analog data transmitter 402.

In a typical implementation, the analog receiver 100 receives and equalizes the analog data signal 102 and optionally converts it to one or more digital data signals 204. The one or more digital data signals 204 are provided to a digital data processor 404, which can include, without limitation, logic, computer program instructions, digital signal processing hardware and/or software, routing hardware and/or software, and the like.

One or more digital data signals 406 are provided to the analog data transmitter 402, which converts the one or more digital data signals 406 to one or more analog data signals 408.

FIG. 5 is a parallel transceiver 500 implementation of the transceiver 400, wherein multiple transceivers 400A-400D are implemented in parallel. Each analog signal 102 is referred to herein as a channel. Thus, the parallel transceiver 500 is referred to herein as a multi-channel transceiver. In an embodiment, multiple parallel transceivers 500 are implemented on a single integrated circuit (IC).

FIG. 6 is a block diagram of the example transceiver 400 implemented as an example multi-gigabit serial analog-to-parallel digital data transceiver 600, including a multi-gigabit serial-to-parallel analog data receiver 602 and a multi-gigabit parallel-to-serial analog data transmitter 604. The multi-gigabit serial-to-parallel transceiver 600 can be implemented as illustrated in FIG. 4 and/or FIG. 5.

FIG. 7 is an example dual-path receiver 700 implementation of the analog data receiver 100. The dual-path receiver 700 includes a data path 702 and a phase path 704. The data path 702 provides data recovery. The phase path 704, in combination with a logic block 706 and a clock control block 708, provides clock recovery and clock control for the data path 702. The phase path 704, the logic block 706, and the clock control block 708, are described in one or more of:

U.S. provisional application titled, :High-Speed Serial Transceiver," serial number 60/200,813, filed April 28, 2000;

U.S. non-provisional patent application titled, "Phase Interpolator Device and Method," serial number (to be assigned), attorney docket number 1875.0560005, filed April 30, 2001;

U.S. non-provisional patent application titled, "Timing Recovery and Phase Tracking System and Method," serial number (to be assigned), attorney docket number 1875.0560002, filed April 30, 2001;

U.S. non-provisional patent application titled, "Timing Recovery and Frequency Tracking System and Method," serial number (to be assigned), attorney docket number 1875.0560001, filed April 30, 2001; and

U.S. non-provisional patent application titled, "High-Speed Serial Data Transceiver and Related Methods," serial number (to be assigned), attorney docket number 1875.0560004, filed April 30, 2001;

all of which are incorporated herein by reference in their entireties.

In an embodiment, the present invention is implemented in a multi-data-path environment including, without limitation, staggered-timing multi-path embodiments. Staggered-timing multi-path embodiments are useful, for example, where the analog data signal 102 is a higher data rate analog signal (e.g., multi-gigabit data rate signal).

For example, FIG. 8 is a block diagram of an example multi-data-path receiver 800 implementation of the analog data receiver 100, including multiple data paths 702A-n. In an embodiment, the multiple data paths 702A-n are operated in a time staggered fashion. Multi-data-path time-staggered operation is useful where, for example, the data rate of the analog data signal 102 is too high for a single data path 702 to handle.

Referring to FIG. 9, in an example staggered sampling embodiment, the multiple data paths 702A-n are provided with example clocking signals 304A-n, which are staggered in time with respect to one another.

Referring back to FIG. 8, in an embodiment, each data path 702A-n includes an optional quantizer 202 (FIG. 2) and each data path 702A-n digitizes a different portion of the analog data signal 102. Outputs of the multiple data paths 702A-n are provided to the logic block 706. The logic block 706 performs sequencing and alignment operations to the outputs from the multiple data paths 702A-n according to an staggered timing scheme. The staggered timing scheme can be any of a variety of conventional staggered timing schemes. In a staggered sampling embodiment, a corresponding phase path 704 is typically provided for each data path 702.

In an embodiment, the present invention is implemented as a signal router. A signal router can be used to route one or more information signals between a plurality of components.

FIG. 10 is an example router 1000, including a front panel 1002, a back plane 1004 and one or more interfacing circuit boards 1006. Front panel 1002 typically includes a plurality of connectors or "jacks," to which external devices, such as computers, servers, terminals, communications devices, other routers, and the like, can be coupled. The router 1000 receives and transmits (i.e., routes) signals, typically between the external devices. The signals can be electrical and/or optical signals.

Each interfacing circuit board 1006 includes a finite number of connections to the front panel 1002 for receiving and/or transmitting signals from/to external devices. Additional interfacing circuit boards 1006 can be utilized to accommodate additional external devices. The backplane 1004 permits the router 1000 to route signals between multiple interfacing circuit boards 1006. In other words, the backplane 1004 permits the router 1000 to route signals between external devices that are coupled to different interfacing circuit boards 1006.

Interfacing circuit boards 1006 can include a variety of digital and/or analog components. When multiple interfacing circuit boards 1006 are utilized, two or more of them can be similar and/or dissimilar. The interfacing circuit boards 1006 illustrated in FIG. 10 are provided for illustrative purposes only. Based on the description herein, one skilled in the relevant art(s) will understand that additional and/or alternative components/features can be provided with the interfacing circuit boards 1006.

Example interfacing circuit board 1006A is now described. Interfacing circuit board 1006A optionally includes one or more interface components 1008 that receive and/or buffer one or more signals received from external devices through the front panel 1002. In the illustrated example, the interface component 1008 receives an optical signal 1010 from the front panel 1002. Accordingly, in this embodiment, interfacing component 1008 includes one or more optical converters that convert the optical signal 1010 to an electrical analog data signal, illustrated here as an analog serial data signal 1012. Additionally, or

alternatively, interfacing component 1008 sends and/or receives one or more other analog data signals 1014A-n to/from other external devices through the front panel 1002. Additionally, or alternatively, interfacing component 1008 sends and/or receives one or more of the signals 1014A-n to/from somewhere other than the front panel 1002.

The serial analog data signal 1012 is provided from the interfacing component 1008 to a transceiver 1010, which can be implemented as one or more of transceivers 400 (FIG. 4), 500 (FIG. 5) and/or 600 (FIG. 6). Transceiver 1010 permits the router 1000 to both receive and transmit analog serial data 1012 from and/or to external devices.

Within the transceiver 1010, one or more receivers 100 equalizes and converts the serial analog data signal 1012 to one or more digital data signals, illustrated here as parallel digital data signals 1016. In an example embodiment, one or more receivers 100 within the transceiver 1010 converts the analog serial data signal 1012 to four ten bit words.

The parallel digital data signals 1016 are optionally provided to a switch fabric 1018, which can be a programmable switch fabric. The optional switch fabric 1018 provides any of a variety of functionalities.

The optional switch fabric 1018 outputs parallel digital data signals 1020 to second transceiver 1022, which can be implemented as one or more of transceivers 400 (FIG. 4), 500 (FIG. 5) and/or 600 (FIG. 6). A transmitter 402 within the transceiver 1022 converts the parallel digital data signals 1020 to serial analog data signals 1024 and transmits them across the back plane 1004 to one or more other interface circuit boards 1006n, and/or back to interface circuit board 1006A.

One or more receivers 100 within the transceiver 1022 receives analog data signals 1024 from the back plane 1004, digitizes them, and converts them to parallel digital data signals 1020. The parallel digital data signals 1020 are provided to the switch fabric 1018, which provides any of a variety of functionalities. The switch fabric 1018 outputs parallel digital data signals 1016

to one or more transmitters 402 within the transceiver 1010, which converts them to analog data signals for transmission to an external devices, possibly through the interface component 1008 and the front panel 1002.

Additional interface circuit boards 1006n operate in a similar fashion. Alternatively, one or more of the interface circuit boards 1006A-n are configured with more or less than the functionality described above. For example, in an embodiment, one or more of the interface circuit boards 1006A-n are configured to receive analog data signals from the front panel 1002 and to provide them to the back plane 1004, but not to receive analog data signals 1024 from the back plane 1004. Alternatively, or additionally, one or more of the interface circuit boards 1006A-n are configured to receive analog data signals 1024 from the back plane 1004 and provide them to the front panel, but not to receive analog data signals from the front panel 1002.

III. Adaptive Equalization Control

In an embodiment, equalization parameters adapt in real time. This permits a receiver to adapt to a variety of signal paths. This also permits multiple parallel receivers to independently adapt to their respective associated signal paths. In FIG. 10, for example, in an embodiment, multiple receivers 100 are implemented within transceiver 1022 for receiving analog signals 1024 from the backplane 1004. Typically, each analog signal 1024 arrives at the transceiver 1022 through a different signal path across the backplane and is thus potentially subject to different inter-symbol distortion. In accordance with the invention, each receiver 100 independently adapts to a respective signal path.

FIG. 14A is an example receiver 1400 implementation of the receiver 100, further including a quality measuring and adaptive control module 1402, which receives the equalized analog data signal 104. The quality measuring and adaptive control module 1402 measures a quality of eye opening of the equalized analog data signal 104 and outputs one or more equalizer control signals 1404.

The equalizer control signals 1404 control one or more parameters in the equalizer 106 to adaptively minimize distortions in the analog data signal 102.

FIG. 14B is an example implementation of the receiver 200, including the optional quantizer 202, the quality measuring and adaptive control module 1402, and an optional digital feedback, illustrated here as the one or more digital signals 204, also referred to herein as hard decisions 204. The hard decision 204 provides the quality measuring and adaptive control module 1402 with additional information from which to measure and/or control the eye opening.

The quality measuring and adaptive control module 1402 can be implemented with analog and/or digital circuits and can be implemented to output analog and/or digital equalizer control signals 1404. Example implementations of the quality measuring and adaptive control module 1402 are described below.

VI. Example Equalizer Embodiments

FIG. 14C is an example embodiment of the receiver 100, wherein the equalizer 106 includes a filter 1410. In an embodiment, the filter 1410 is a high data rate filter.

Generally, high data rate filters are expensive to implement. However, the present invention provides filtering methods and systems, including adaptive hybrid analog/digital high frequency filtering methods and systems, that are uncomplicated and inexpensive to implement.

For example, FIG. 14D is an example embodiment of the receiver 100, wherein the filter 1410 includes one or more finite impulse response ("FIR") filters 1412.

In an embodiment, the one or more FIR filters 1412 are implemented as analog FIR filters. For example, FIG. 14E is an example implementation of the receiver 100 wherein the FIR filter 1412 includes one or more analog FIR filters 1414. FIGS. 14F and 14G illustrate example implementations of the one or more analog FIR filters 1414.

V. Discreet-Time Analog Equalization

In an embodiment, the present invention equalizes discreet-time analog samples of the analog data signal 102.

Referring to FIG. 14H, the one or more FIR filters 1412 are implemented as one or more discreet-time analog FIR filters 1416.

Referring to FIG. 15, the equalizer 106 is illustrated with a sampler 1500 that samples the analog data signal 103 and outputs discreet-time analog samples 1502. In an embodiment, the sampler 1500 includes one or more sample and hold and/or a track and hold circuits. In FIG. 15, the sampler 1500 is illustrated as part of the equalizer 1400. Alternatively, the sampler 1500 can be outside of the equalizer 1400.

In operation, the sampler 1500 samples the analog data signal 102 in accordance with the Nyquist theorem and the discreet-time analog FIR 1502 operates on discreet-time analog samples 1504 of the analog data signal 102.

When the receiver 100 is implemented with one or more discreet-time filters 1416 and the optional quantizer 202, the quantizer 202 generally has better sensitivity because the discreet-time analog samples can be quantized over a longer period of time. Thus even a very low voltages can be detected by quantizer.

The discreet-time analog FIR filter 1416 can be implemented in any of a variety of ways. FIG. 19 is a block diagram of an example single tap implementation of the discreet-time analog FIR filter 1416. Additional taps can also be implemented.

In FIG. 19, the discreet-time analog FIR filter 1416 includes a fixed weight 1920 that operates on a present output of the sampler 1500. The discreet-time analog FIR filter 1416 further includes a tap defined by a delay 1922 and an adjustable weight 1924. The adjustable weight 1924 operates on a prior output of the sampler 1500. The fixed weight 1920 and the variable weight 1924 scale

the present output of the sampler and the prior output of the sampler, respectively, according to values of the respective weights.

The output of the adjustable weight 1924 is subtracted from the output of the first weight 1920 in a combiner 1926.

FIG. 16 is an example discreet-time analog dual path receiver 1600 implementation of the receiver 100, including the sampler 1500, the discreet-time analog FIR filter 1416, and optional quantizer 202.

In FIG. 16, the phase path 704 provides clock recovery for the sampler 1500 and the data path 702 so that the sampler 1500 and the quantizer 202 operate at the correct frequency and phase of the analog data signal 102.

FIG. 17 is an example discreet-time analog dual path receiver 1700 implementation of the receiver 1600, wherein the phase path 704 includes a phase detector 1702, a loop filter 1704, and a phase/frequency adjust/correct block 1706.

Phase path 702 preferably takes into account any path delay in the data path 702. One way to take into account delay in data path 702 is to determine the path delay in the data path 702 and design the phase path 704 accordingly.

Alternatively, the data path 702 and the phase path 704 are made substantially similar to one another so that they have substantially similar path delays. In such an embodiment, phase and frequency correction developed by the phase path 704 inherently corrects for any path delay in the data path 702.

For example, FIG. 18 is an example dual path receiver 1800 implementation of the receiver 1600, wherein the equalizer 106 forms part of the data path 702 and the phase path 704 so that at least the front end of data path 702 and the front end of phase path 704 are substantially similar to one another.

VI. Example Implementations of the Quality Measuring and Adaptive Control Module

FIG. 20 is a high level block diagram of an example implementation of the quality measuring and adaptive control module 1402 (FIG. 14H), including a measuring module 2002 and an equalizer control module 2006. Measuring module 2002 is implemented with analog and/or digital circuitry. Similarly, equalizer control module 2004 is implemented with analog and/or digital circuitry.

Where the measuring module 2002 is implemented with digital circuitry, an optional analog-to-digital converter ("ADC") 2004 converts the equalized analog data signal 104 to a multi-level digital representation 2008 of the equalized analog data signal 104, for use by the measuring module 2002. The multi-level digital representation 2008 is also referred to herein as a soft decision 2008.

Alternatively, digital conversion can be performed within the measuring module 2002, between the measuring module 2002 and the equalizer control module 2006, or within the equalizer control module 2006. Alternatively, where the quality measuring and adaptive control module 1402 is implemented entirely with analog components, the optional ADC 2004 is omitted.

In a discreet-time analog embodiment, the optional ADC 2004 can be operated at a sub-sample rate with respect to the sampler 1500. In other words, the ADC 1904 operates on fewer than every equalized sample from the discreet-time analog FIR filter 1416. For example, in an embodiment, the ADC 2004 operates on every eighth equalized sample from the discreet-time analog FIR filter 1416.

Alternatively, in order to avoid lock-up on certain data patters, the ADC 2004 sub-sample rate is periodically changed to one or more other sub-sample rates. For example, the ADC 2004 can be operated at a first sub-sample rate (e.g. 1/8) for a period of time and then operated at a second sub-sample rate (e.g. 1/7) for another period of time. Following that, operation of the ADC 2004 can revert back to the first sub-sample rate or can be changed to a third sub-sample rate. Any number of different sub-sample rates and/or periods can be utilized.

Changes to the sub-sample rate and/or the periods that the sub-sample rates are utilized can be the same or different. Changes to the sub-sample rates and/or periods can be random or ordered.

The invention is not, however, limited to these example embodiments. Based on the description herein, one skilled in the relevant art(s) will understand the ADC 2004 can operate on every equalized sample from the FIR filter 1502, or any subset and/or off-set thereof.

In an embodiment, the quality measuring and adaptive control module 1402 can be implemented to output one or more analog and/or digital equalizer control signals 1404. Where the quality measuring and adaptive control module 1402 is implemented to output one or more digital equalizer control signals 1404, the invention essentially provides digitally controlled equalization of an analog data signal.

Where the quality measuring and adaptive control module 1402 is implemented to output one or more digital equalizer control signals 1404, and the equalizer includes a discreet-time analog FIR filter 1416 (FIGS. 14H and 15), the invention essentially provides digitally controlled equalization of a discreet-time analog data signal.

In an embodiment, the receiver 100 includes the optional quantizer 202, , the quality measuring and adaptive control module 1402 optionally receives the digital data signal 204, and the quality measuring and adaptive control module 1402 compares the equalized analog data signal 104 with the digitized data signal 204. In an example implementation of such an embodiment, the measuring and adaptive control module 1402 utilizes a least-means-squared ("LMS") algorithm to adaptively control the equalizer 106. For example, the LMS algorithm can provide tap updates for the FIR filter 1412. Any of a variety of conventional LMS methods and/or systems can be utilized.

Where the quality measure and adaptive control module 1402 receives the equalized analog data signal 104 and the hard decision 204, the quality measure and adaptive control module 1402 optionally converts the equalized analog data

signal 104 to the soft decision 2008 to compare it with the hard decision 204, utilizing, for example, the LMS algorithm.

Alternatively, the quality measuring and adaptive control module 1402 compares the equalized analog data signal 104 to the hard decision 204 without converting the equalized analog data signal 104 to a digital soft decision.

The present invention is not limited to LMS embodiments.

In an embodiment, the quality measuring and adaptive control module 1402 generates equalizer control signals 1410 without utilizing feedback from the quantizer 202.

FIGS. 21A, B, C and D illustrate an example implementation of the receiver 100. FIG. 21A illustrates example implementations of the measuring module 2002 and the ADC 2004. FIGS. 21B and 21C illustrate example implementations of the equalizer control module 2006. FIG. 21D is an example state diagram 2108 for implementing a state machine 2106 illustrated in FIGS. 21B and 21C. Operation of these example embodiments are now described.

Referring to FIG. 21A, the measuring module 2002 receives the equalized analog data signal 104. An amplitude module 2101 measures an amplitude of the equalized analog data signal 104. In an embodiment, the amplitude module 2101 determines absolute amplitudes of the equalized analog data signal 104.

A control logic module 2112 determines whether a portion of the equalized analog data signal 104 is a steady state soft portion or a post-transition portion.

A switching system 2110 directs the amplitudes of the equalized analog data signal 104 to a transition path 2114 or a no-transition path 2116, according to controls from the control logic module 2112. In an embodiment, the control logic module 2112 is part of the phase path 704.

Transition path 2114 and no-transition path 2116 sample and integrate the amplitudes of the equalized analog data signal 104 to obtain average values of post-transition and steady state portions, respectively. A combiner 2118 outputs

an average difference 2120 between the average post-transition and steady state values.

The average difference 2120 is provided to the ADC 2004, which outputs a digital representation 2122 of the average difference 2120. In an embodiment, the ADC 2004 is implemented as a high/med/low system that compares the average difference 2120 with a plurality of pre-determined values, whereby the ADC 2004 outputs a thermometer code that indicates which, if any, of the plurality of pre-determined values are exceeded by the average difference 2120.

Referring to FIG. 21B, the digital representation 2122 is provided to the state machine 2106. In an embodiment, the state machine 2106 samples the digital representation 2122 at a pre-determined rate. The state machine 2106 determines whether a current equalization factor (e.g., variable weight 1924 in FIG. 19) is too high, too low, or adequate. Depending upon the determination, the state machine 2106 will increase, decrease or maintain the current equalization factor. Appropriate tap updates are provided by the state machine 2106 as equalizer control signals 1404.

The elements described above can be implemented in hardware, software, firmware, and combinations thereof. The elements described above can be implemented with analog and/or digital circuits. For example, integration can be performed digitally with accumulators.

C. Transconductors

In an embodiment, the invention utilizes transconductors, or current sources. For example, in an embodiment of the discreet-time analog system FIG. 19, the fixed weight 1920 and the adjustable weight 1924 are implemented with transconductors. Furthermore, the discreet-time analog FIR filter 1416 is implemented with differential signals, including "plus" and "minus" differential signals for example. The combiner 2008 is then implemented by coupling the plus output from the fixed weight 1920 with the minus output of the variable

weight 1924 and by coupling the minus output from the fixed weight 1920 with the plus output of the variable weight 1924.

The example implementations of the discreet-time analog FIR filter 1416 described and illustrated herein are provided for illustrative purposes only. Based on the description herein, one skilled in the relevant art(s) will understand that the discreet-time analog FIR filter 1416 can be implemented in a variety of other ways. For example, and without limitation, additional taps can be utilized, fixed weight 1920 can be replaced with an adjustable weight, and/or variable weight 1924 can be replaced with a fixed weight. Where the discreet-time analog FIR filter 1416 is implemented with fixed weights only, the equalizer 106 is referred to herein as a fixed-weight equalizer.

VII. Multi-Path Adaptive Equalization

FIG. 22 is an example discreet-time analog multi-path receiver 2200 where the data paths 702A-n are operated in a time-staggered fashion, for example by the clock signals 304A-n (FIG. 9). The clock signals 304A-n operate the samplers 1500A-n in staggered fashion so that data path n-1 samples the analog data signal 102 prior to the data path n. In this embodiment, the delay elements 1922 (FIG. 19) are omitted and the input to the variable weights 1924A-n are provided by the sampler 1500 in an adjacent data path 702, which sampled at a prior time. For example, variable weight 1924B in data path 702B receives samples from sampler 1500A in data path 702A.

Multi-path embodiments can be implemented to control the discreet-time analog FIR filter 1416 based on the equalized analog data signal 104 and/or the digital data signal 204, as described above.

In a discreet-time analog multi-path receiver embodiment, one or more quality measure and adaptive control modules 1402 can be utilized. For example, in FIG. 22, a single quality measure and adaptive control module 1402 receives equalized analog data signal 104 and optionally receives digital data

signal 204, from a single data path 702A. Alternatively, separate quality measure and adaptive control modules 1402 are implemented for each data path 702.

Where four data paths 702A-D are implemented, and where the quality measure and adaptive control module 1402 operates on every eighth sample of the equalized analog data signal 104A, as described above, the quality measure and adaptive control module 1402 effectively operates on every thirty-second sample of the analog data signal 102.

The invention is not, however, limited to these example embodiments. Based on the description herein, one skilled in the relevant art(s) will understand that other embodiments can be implemented. For example, any number of data paths 702 can be implemented. Also, the quality measure and adaptive control module 1402 can operate on every sample of the equalized analog data signal 104A, or any sub-set thereof. Similarly, the quality measure and adaptive control module 1402 can operate on samples from other data paths 702 B-n in addition to and/or alternative to the samples from data path 702A.

In an embodiment, the discreet-time analog multi-path receiver 2200 automatically switches between single data path operation and staggered multi-path operation depending upon the data rate, without user input.

In an embodiment, the discreet-time analog multi-path receiver 2200 utilizes transconductances, or current sources, as described above.

VII. Implementation in the Example Environments

One or more receivers in accordance with the invention can be implemented in any of the example environments illustrated in FIGS. 1-10. However, the invention is not limited to the example environments.

Referring to FIG. 10, for example, one or more receivers 100, implemented in accordance with the invention, can be implemented as part of the router 1000. For example, in an embodiment, transceiver 1022 includes a plurality of receivers 100, implemented in accordance with the present invention,

wherein each receiver 100 receives a different one of the analog data signals 1024 from the backplane 1004. Each receiver 100 adapts to the signal path associated with its respective analog data signal 1024, in accordance with the invention.

In an embodiment, one or more transceivers 1010 and/or 1022 in accordance with the present invention are implemented on an application specific integrated circuit ("ASIC") that includes the switch fabric 1018.

In an embodiment, one or more receivers according to the present invention are implemented on an integrated circuit ("IC") chip.

In an embodiment, one or more multi-path receivers according to the present invention are implemented on an integrated circuit ("IC") chip.

For example, FIG. 23 is an example IC chip 2302 including a plurality of multi-path receivers 2304A-m, each multi-path receiver 2304A-m having multiple data paths 2306A-n. "n" and "m" can be equal or different. In an embodiment, "n" and "m" equal four. The multi-path receivers 2304A-m can have different numbers of data paths 2306.

The IC chip 2302 can be implemented as one or more of the receivers 100 in the router 1000 illustrated in FIG. 10. For example, in an embodiment, the IC chip 2300 includes transceiver 1022 in FIG. 10, wherein each receiver 2304 receives a different one of the analog data signals 1024 from the backplane 1004. Each of the analog data signals 1024 travels through the backplane 1004 through a different path and thus potentially have different inter-symbol distortions. Accordingly, each of the receivers 2304 will adapt to the signal path associated with its respective analog data signal 1024.

In an embodiment, IC chip 2302 further the switch fabric 1018.

IX. Example Methods for Adaptive Equalization

FIG. 24 is an example process flowchart 2400 for adaptively equalizing an analog information signal for a given signal path. In an embodiment, the analog information signal is a higher data rate analog information signal.

Alternatively, the analog information signal is a lower data rate analog information signal.

FIG. 25 is an example process flowchart 2500 for implementing step 2404 in the flowchart 2400.

In an embodiment, steps 2502-2508 are performed at a sub-sample rate relative to the sampling of step 2402.

In an embodiment, steps 2502-2508 are performed at an off-set of a sub-sample rate relative to the sampling of step 2402.

FIG. 26 is an example process flowchart 2600 for implementing step 2404 in the flowchart 2400.

In an embodiment, step 2602 is are performed at a sub-sample rate relative to the sampling of step 2402.

In an embodiment, step 2602 is are performed at an off-set of a sub-sample rate relative to the sampling of step 2402.

FIG. 27 is an example process flowchart 2700 for implementing step 2602 in the flowchart 2600.

In an embodiment, steps 2704, 2706 and 2708 are performed by averaging.

In an embodiment, steps 2704, 2706 and 2708 are performed by accumulating.

FIG. 28 is an example process flowchart 2800 for adaptively equalizing time-staggered portions of an analog information signal for a given signal path.

In an embodiment, step 2804 is performed at a sub-sample rate relative to the sampling of step 2802.

In an embodiment, step 2804 is performed at an off-set of a sub-sample rate relative to the sampling of step 2802.

In an embodiment, the flowchart 2800 performed with one or more of the steps illustrated in one or more of the flowcharts 2500-2700.

FIG. 29 is an example process flowchart 2900 for adaptively equalizing time-staggered portions of a plurality of analog information signals for their respective signal paths.

In an embodiment, step 2908 is performed at a sub-sample rate relative to the sampling of step 2902.

In an embodiment, step 2908 is performed at an off-set of a sub-sample rate relative to the sampling of step 2902.

In an embodiment, the flowchart 2900 performed with one or more of the steps illustrated in one or more of the flowcharts 2500-2700.

FIG. 30 is an example process flowchart 3000 for adaptively equalizing a plurality of analog information signals for their respective signal paths.

In an embodiment, step 3006 is performed at a sub-sample rate relative to the sampling of step 2002.

In an embodiment, step 3006 is performed at an off-set of a sub-sample rate relative to the sampling of step 2002.

In an embodiment, the flowchart 3000 performed with one or more of the steps illustrated in one or more of the flowcharts 2500-2700.

X. Conclusions

The present invention has been described above with the aid of functional building blocks illustrating the performance of specified functions and relationships thereof. The boundaries of these functional building blocks have been arbitrarily defined herein for the convenience of the description. Alternate boundaries can be defined so long as the specified functions and relationships thereof are appropriately performed. Any such alternate boundaries are thus within the scope and spirit of the claimed invention. One skilled in the art will recognize that these functional building blocks can be implemented by discrete components, application specific integrated circuits, processors executing appropriate software and the like or any combination thereof.

While various embodiments of the present invention have been described above, it should be understood that they have been presented by way of example only, and not limitation. Thus, the breadth and scope of the present invention should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

WHAT IS CLAIMED IS:

1. A method for adaptively equalizing a multi-gigabit analog information signal for a signal path, comprising the steps of:

(1) sampling a multi-gigabit analog information signal;

(2) performing an equalizing process on the samples; and

(3) quantizing the equalized samples of the multi-gigabit analog information signal.

2. The method according to claim 1, wherein step (2) comprises the steps of:

(a) comparing a multi-level representation of the equalized samples with the quantized equalized samples;

(b) performing a least-means-squared operation on results of the comparison;

(c) adjusting an equalization coefficient with a result of the least-means-squared operation; and

(d) repeating steps (2)(a) through (2)(c).

3. The method according to claim (2), wherein steps (2)(a) through (2)(d) are performed at a sub-sample rate relative to the sampling of step (1).

4. The method according to claim (2), wherein steps (2)(a) through (2)(d) are performed at a an off-set of a sub-sample rate relative to the sampling of step (1).

5. The method according to claim 1, wherein step (2) comprises the steps of minimizing differences between post-transition sample amplitudes and steady state sample amplitudes of the samples.

6. The method according to claim 5, wherein step (2) comprises the steps of:

(a) distinguishing between post-transition samples and steady-state samples;

(b) integrating post-transition sample amplitudes;

(c) integrating steady-state sample amplitudes;

(d) determining a difference between the integrated post-transition sample amplitudes and the integrated steady-state sample amplitudes;

(e) adjusting an equalization coefficient to minimize the differences between the integrated post-transition sample amplitudes and the integrated steady-state sample amplitudes; and

(f) repeating steps (2)(a) through (2)(e).

7. The method according to claim (6), wherein steps (2)(a) through (2)(f) are performed at a sub-sample rate relative to the sampling of step (1).

8. The method according to claim (6), wherein steps (2)(a) through (2)(f) are performed at a an off-set of a sub-sample rate relative to the sampling of step (1).

9. The method according to claim 5, wherein step (2) comprises the steps of:

(a) distinguishing between post-transition samples and steady-state samples;

(b) averaging post-transition sample amplitudes;

(c) averaging steady-state sample amplitudes;

(d) determining a difference between the averaged post-transition sample amplitudes and the averaged steady-state sample amplitudes;

(e) adjusting an equalization coefficient to minimize the differences between the integrated post-transition sample amplitudes and the integrated steady-state sample amplitudes; and

(f) repeating steps (2)(a) through (2)(e).

10. The method according to claim 5, wherein step (2) comprises the steps of:

(a) distinguishing between post-transition samples and steady-state samples;

(b) accumulating post-transition sample amplitudes;

(c) accumulating steady-state sample amplitudes;

(d) determining a difference between the accumulated post-transition sample amplitudes and the accumulated steady-state sample amplitudes;

(e) adjusting an equalization coefficient to minimize the differences between the integrated post-transition sample amplitudes and the integrated steady-state sample amplitudes; and

(f) repeating steps (2)(a) through (2)(e).

11. The method according to claim 1, wherein step (2) comprises the step of minimizing inter-symbol interferences in the samples.

12. The method according to claim 1, wherein step (2) comprises the step of minimizing inter-symbol interferences in the samples.

13. A method adaptively equalizing time staggered portions of a multi-gigabit analog information signal for a signal path, comprising the steps of:

(1) sampling the multi-gigabit analog information signal at a plurality of phases;

(2) measuring an equalization quality of the samples from one of the plurality of phases;

(3) equalizing the samples from each of the phases based on the measured equalization quality of the one phase; and

(3) quantizing the equalized samples.

14. A method for adaptively equalizing a time-staggered portions of a plurality of multi-gigabit analog information signals for respective signal paths, comprising the steps of:

(1) generating clock signals from the plurality multi-gigabit analog information signals;

(2) sampling each of the multi-gigabit analog information signals at a plurality of phases of the respective clock signals;

(3) measuring an equalization quality of the samples from one of the plurality of phases for each of the multi-gigabit analog information signals;

(4) equalizing the samples from each of the phases of each of the multi-gigabit analog information signals based on the measured equalization quality of the one phase of each of the respective multi-gigabit analog information signals; and

(5) quantizing the equalized samples.

15. A method for adaptively equalizing a plurality multi-gigabit analog information signals for respective signal paths, comprising the steps of:

(1) generating a clock signal for each of the multi-gigabit analog information signals from each of the respective multi-gigabit analog information signals;

(2) sampling each of the multi-gigabit analog information signals according to the respective clock signals;

(3) performing an equalizing process on the samples; and

(5) quantizing the equalized samples.

16. A system for quantizing a multi-gigabit serial analog information signal, comprising:

a sampler;

an equalizer coupled to said sampler; and

a quantizer coupled to said equalizer;

wherein said equalizer minimizes inter-symbol interferences in samples output from said sampler and said quantizer quantizes equalized samples output from said equalizer.

17. The system according to claim 16, wherein said equalizer comprises an finite impulse response filter ("FIR") having at least one adjustable tap, said system further comprising control logic coupled to said FIR, wherein said control logic generates tap updates for said FIR.

18. The system according to claim 17, wherein said control logic comprises:

a first input coupled to an output of said equalizer;

an analog-to-digital converter ("ADC") coupled to said first input; and

a control module coupled to an output of said ADC;

wherein said ADC generates multi-level representations of equalized samples, and said control module generates said tap updates from at least said multi-level representations of the equalized samples.

19. The system according to claim 17, wherein s aid control logic comprises:

a second input coupled to an output of said quantizer; and

a least-means-squared ("LMS") module coupled to said first and second control logic inputs;

wherein said LMS module compares the multi-level representations of equalized samples with the quantized samples from said quantizer and generates said tap updates according to the comparison.

20. The system according to claim 17, wherein said control logic comprises:

a difference detector having a steady-state path, a post-transition path, and a combiner; and

a state machine coupled to one or more outputs of said difference detector;

wherein said combiner outputs an average difference between post-transition amplitudes of the equalized samples and steady-state amplitudes of the equalized samples, wherein said state machine generates said tap updates according to said average difference.

21. A system for routing and adaptively equalizing high data rate analog data signals, comprising:

a backplane having a plurality of signal paths; and

at least one interface board coupled to said backplane, said interface board including a plurality of receivers coupled to said backplane signal paths, each said receiver including an adaptive equalizer;

wherein each said equalizer adapts to an associated backplane signal path to equalize an analog data signal received from said associated backplane signal path.

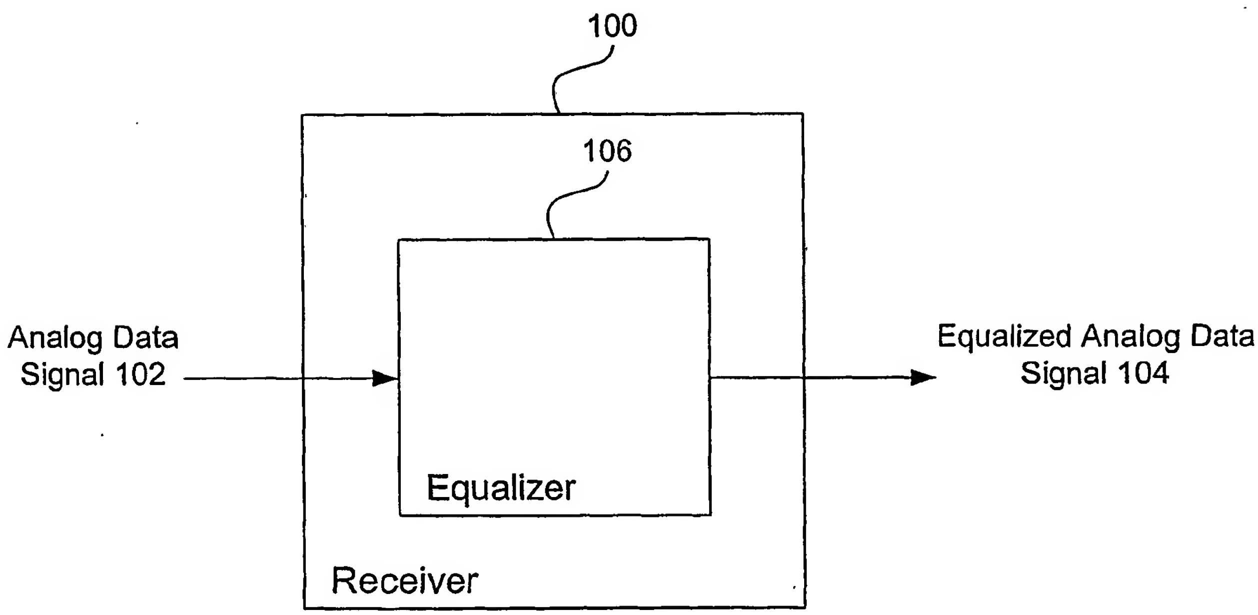

100
106
Analog Data
Signal 102
Equalizer
Receiver
Equalized Analog Data
Signal 104

FIG. 1

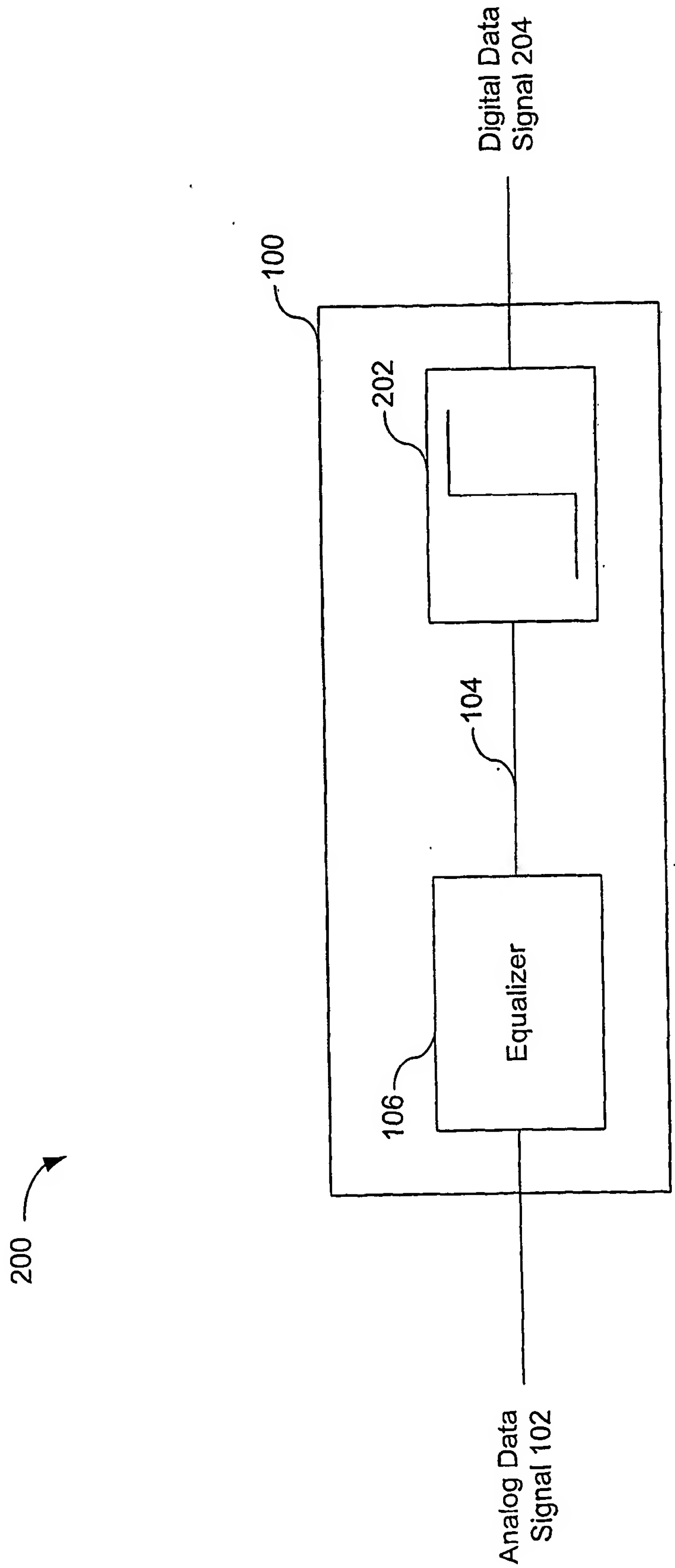
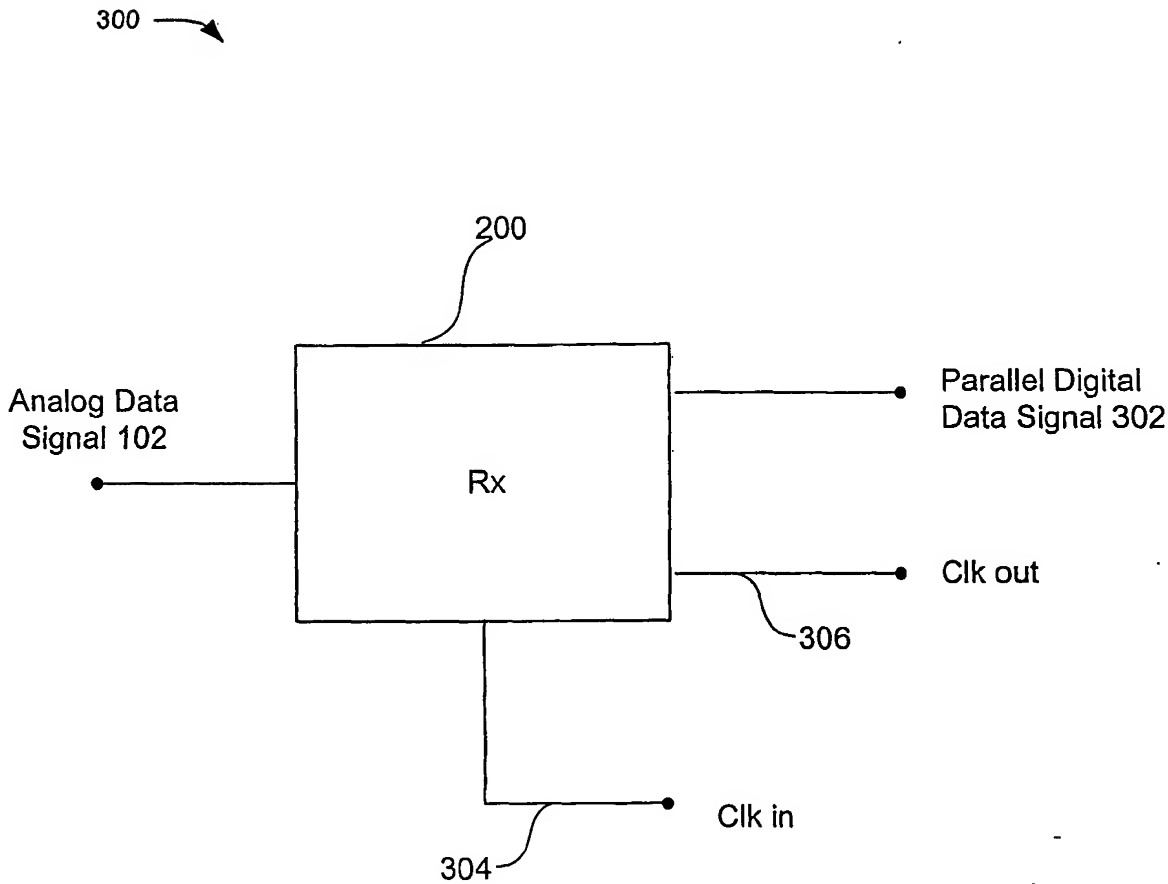

Digital Data
Signal 204
100
202
104
Equalizer
106
200
Analog Data
Signal 102

FIG. 2



Serial-to-Parallel Receiver

FIG. 3

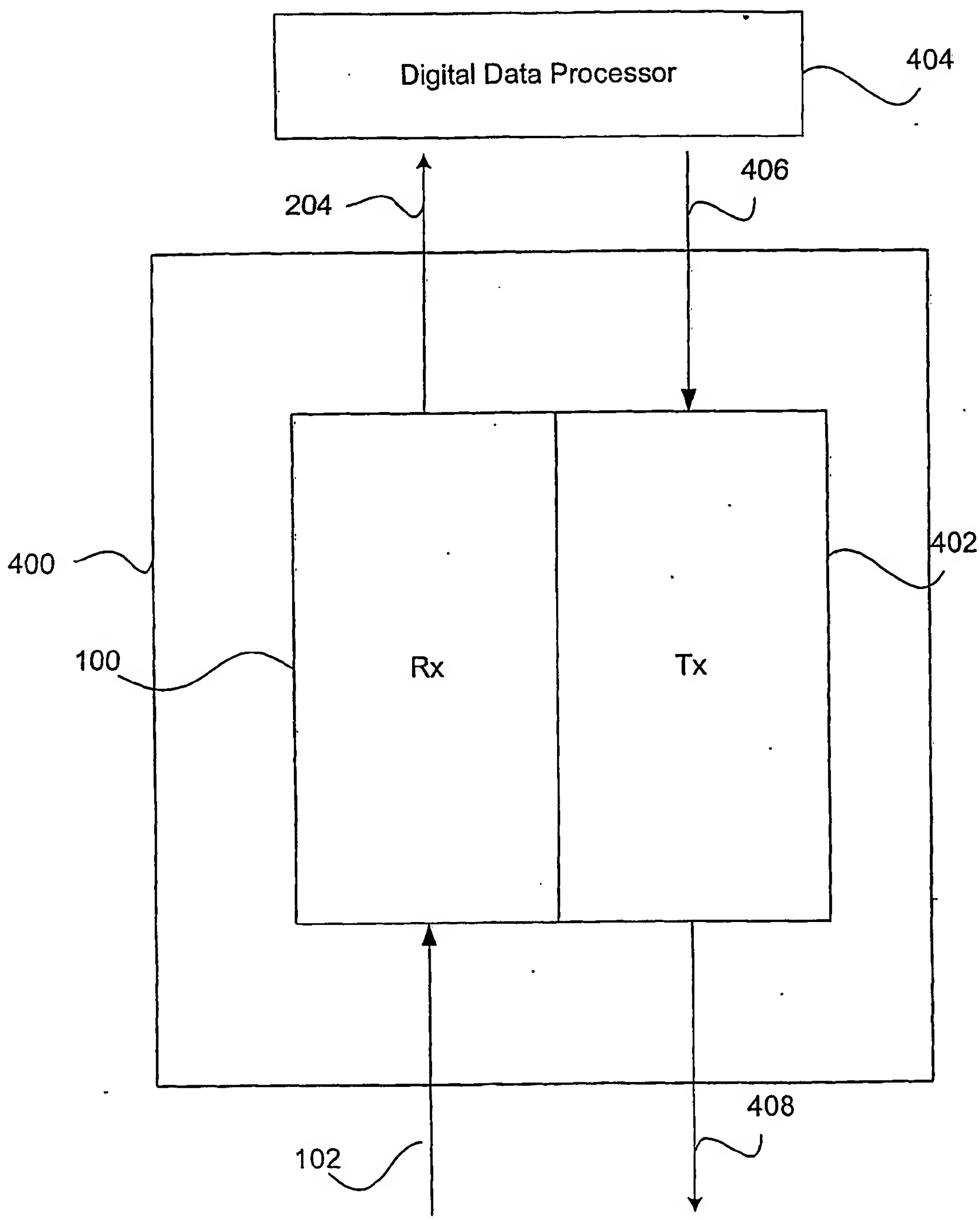


FIG. 4

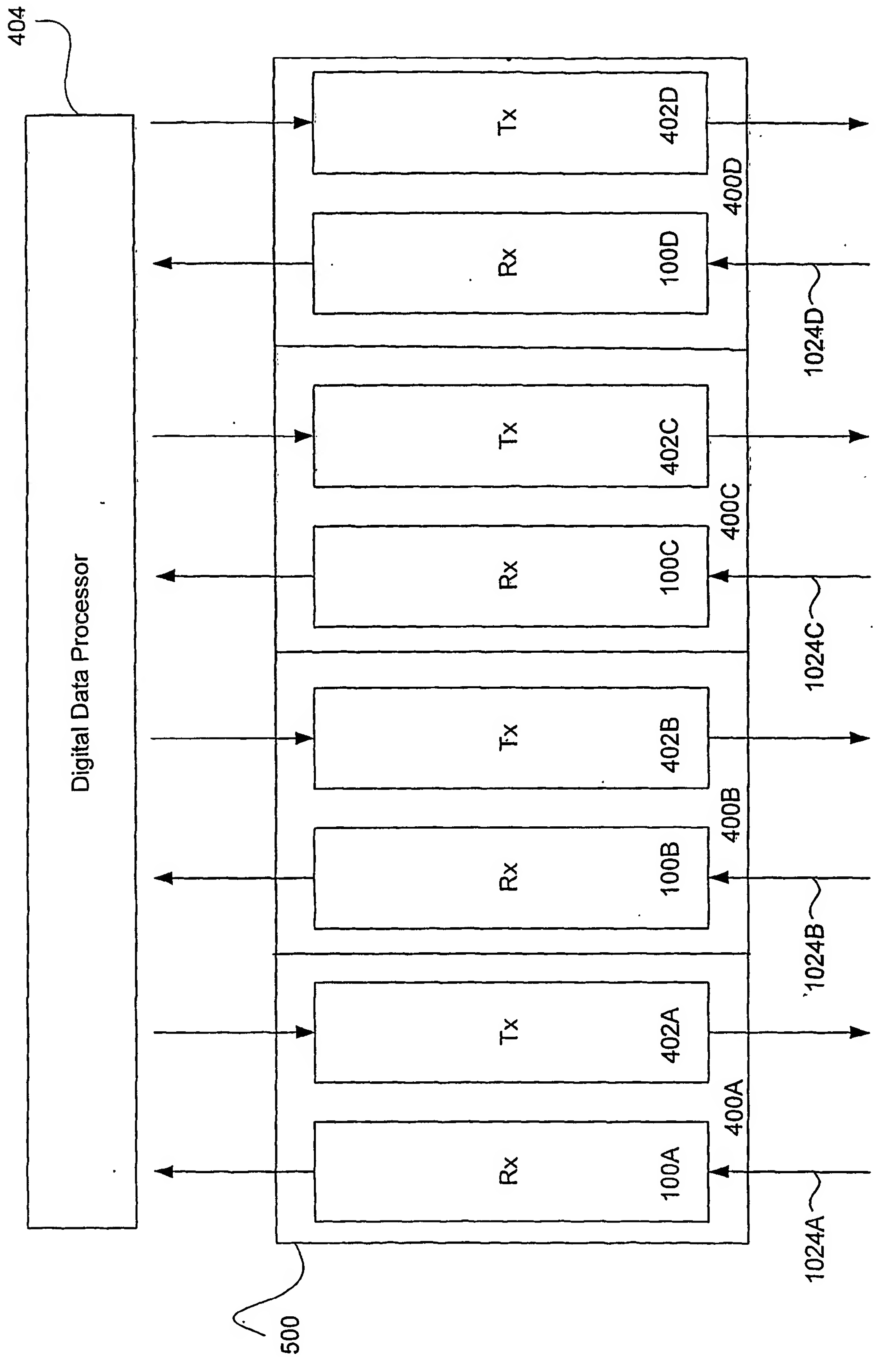

404
Digital Data Processor
Tx
402D
Rx
100D
400D
1024D
Tx
402C
Rx
100C
400C
1024C
Tx
402B
Rx
100B
400B
1024B
Tx
402A
Rx
100A
400A
1024A
500

FIG. 5

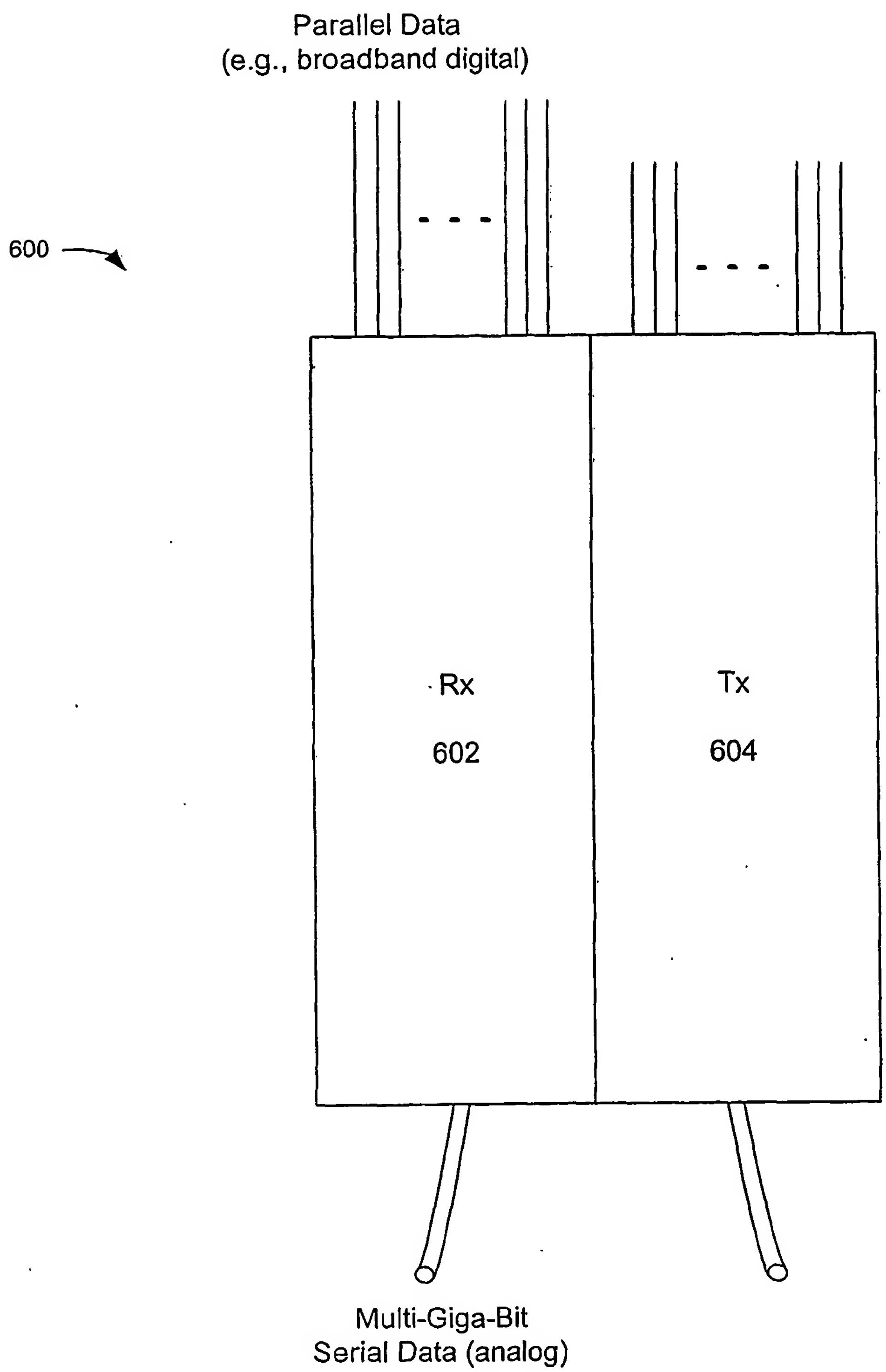

Parallel Data
(e.g., broadband digital)
600
Rx
602
Tx
604
Multi-Giga-Bit
Serial Data (analog)

FIG. 6

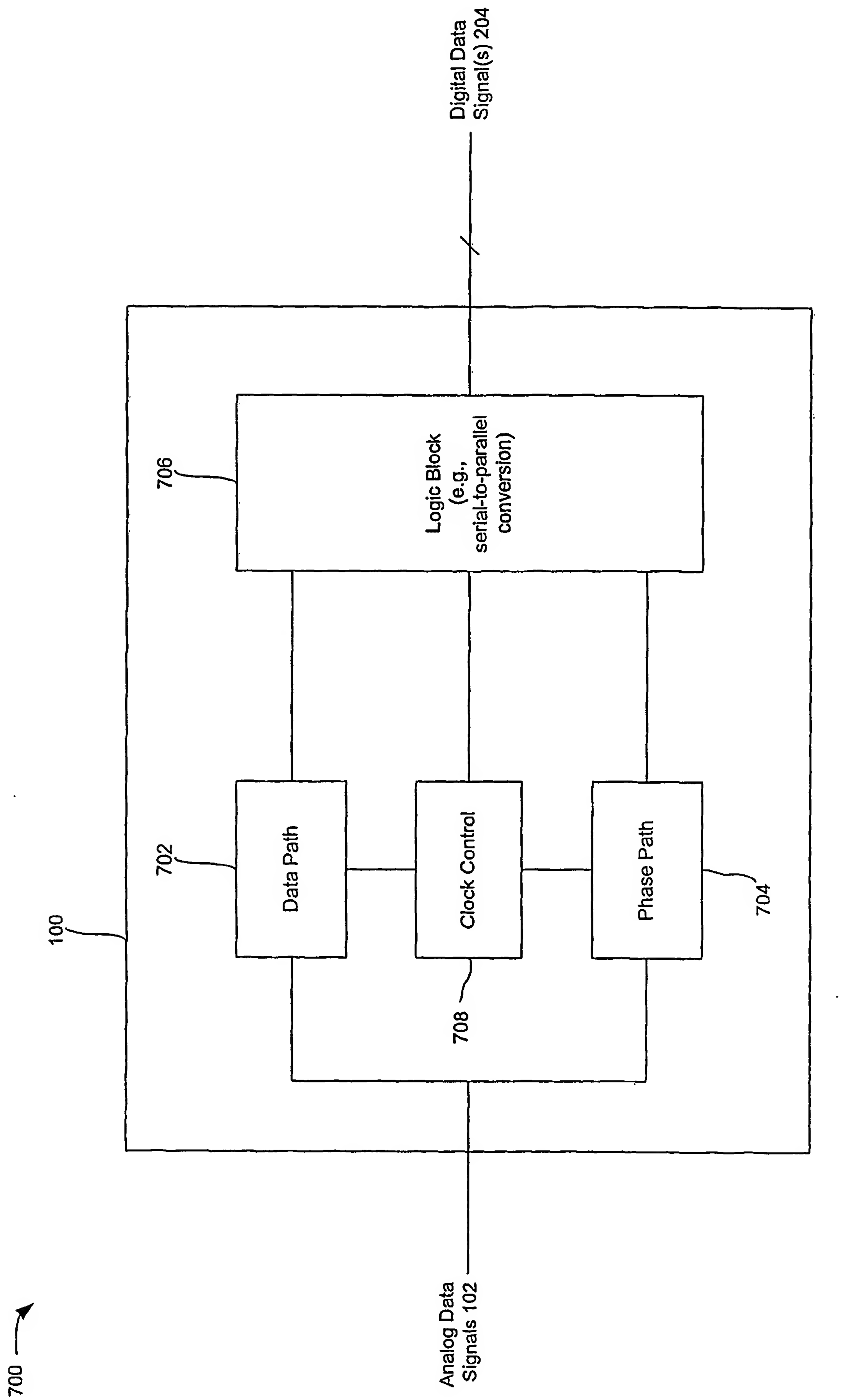

Digital Data Signal(s) 204
Logic Block (e.g., serial-to-parallel conversion)
706
Data Path
702
Clock Control
708
Phase Path
704
100
Analog Data Signals 102
700

FIG. 7

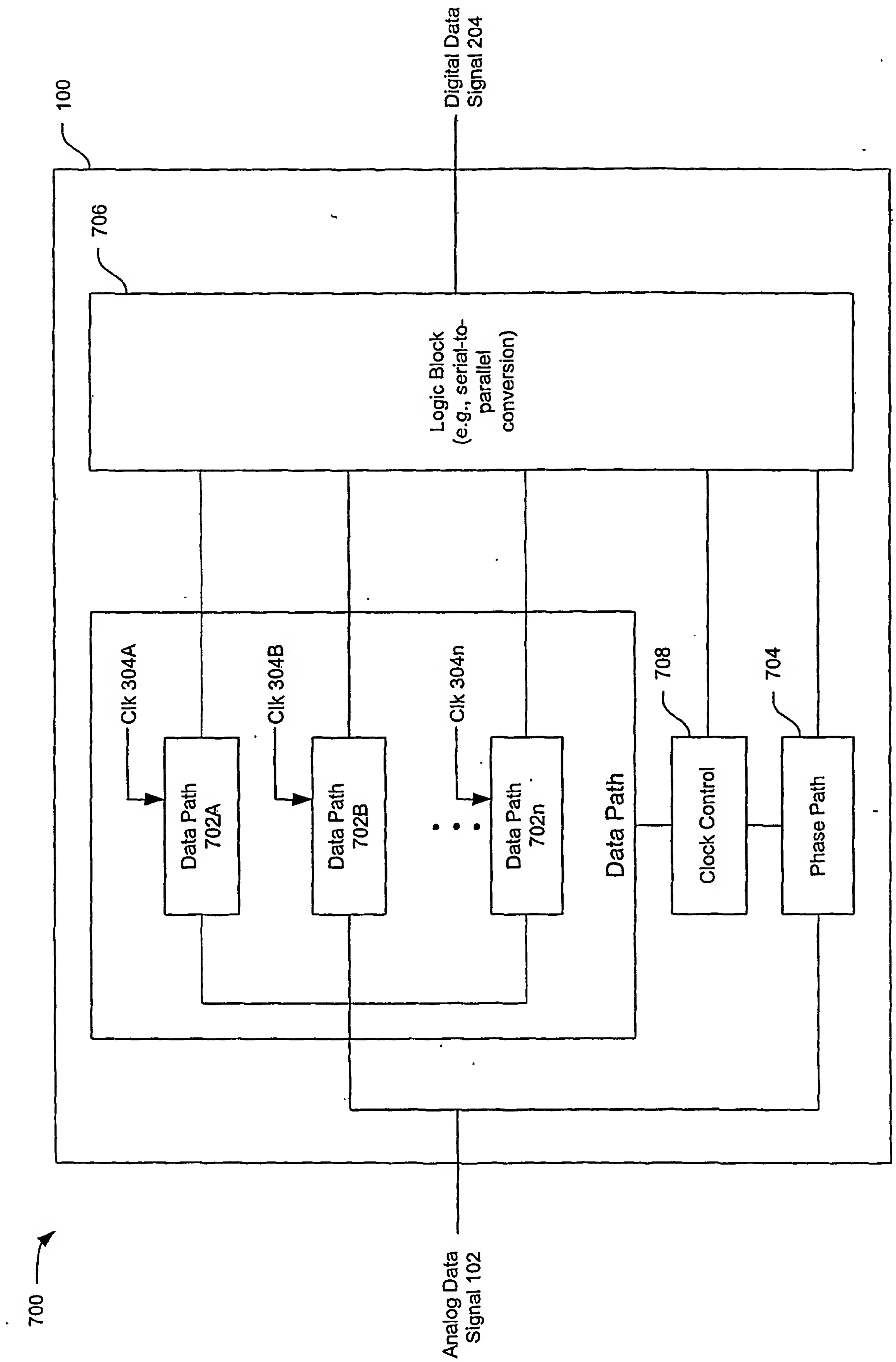

100
Digital Data Signal 204
706
Logic Block (e.g., serial-to-parallel conversion)
Clk 304A
Clk 304B
Clk 304n
Data Path 702A
Data Path 702B
Data Path 702n
Data Path
708
Clock Control
704
Phase Path
700
Analog Data Signal 102

FIG. 8

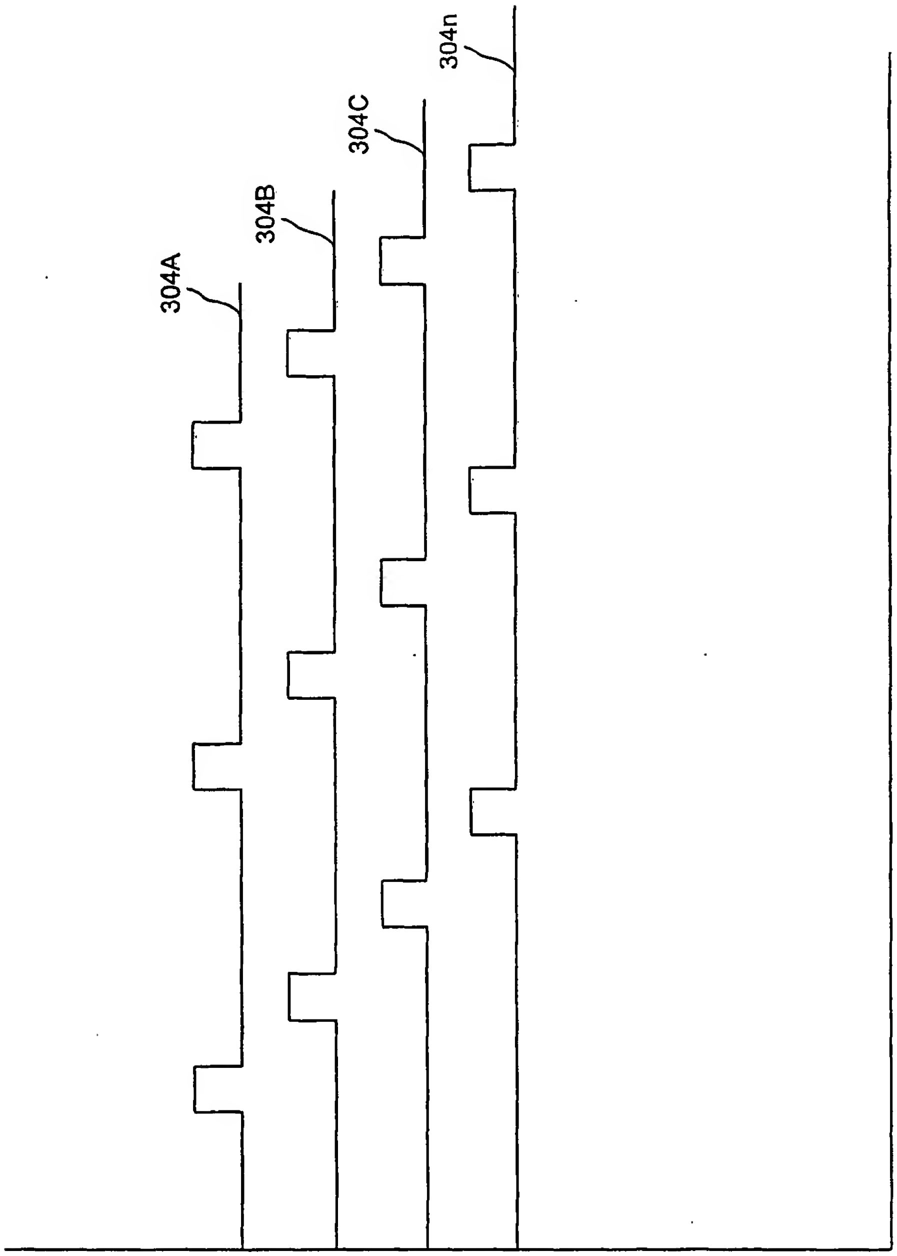


FIG. 9

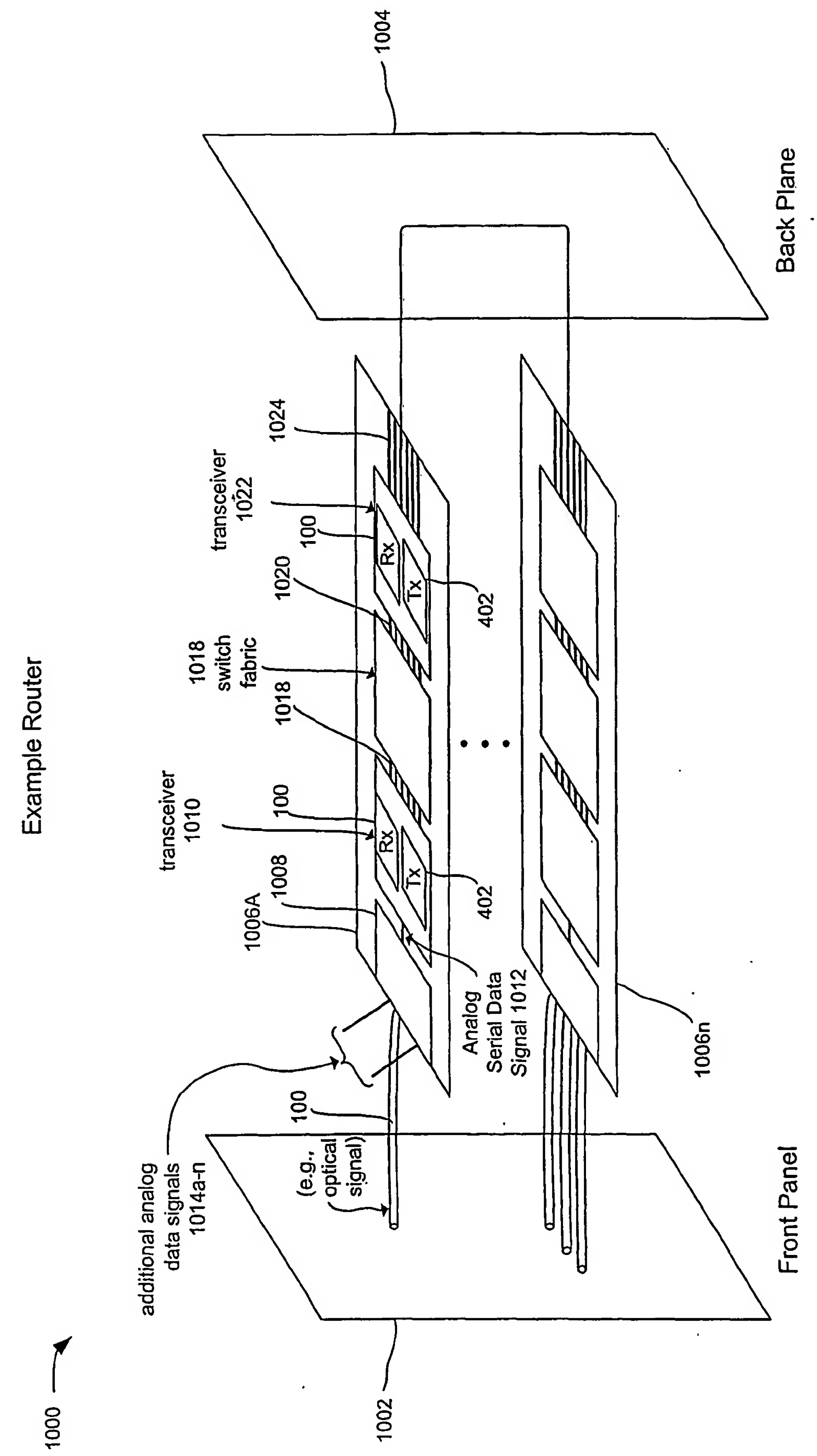

1000
Example Router
1002
1004
Front Panel
Back Plane
additional analog data signals 1014a-n
(e.g., optical signal)
100
1006A
1008
Analog Serial Data Signal 1012
transceiver 1010
100
Rx
Tx
402
1018
1018 switch fabric
1020
transceiver 1022
100
Rx
Tx
402
1024
1006n

FIG. 10

Receiver Eye Diagrams: 3.125-Gb/s

Backplane
36-inches FR4
No Equalization

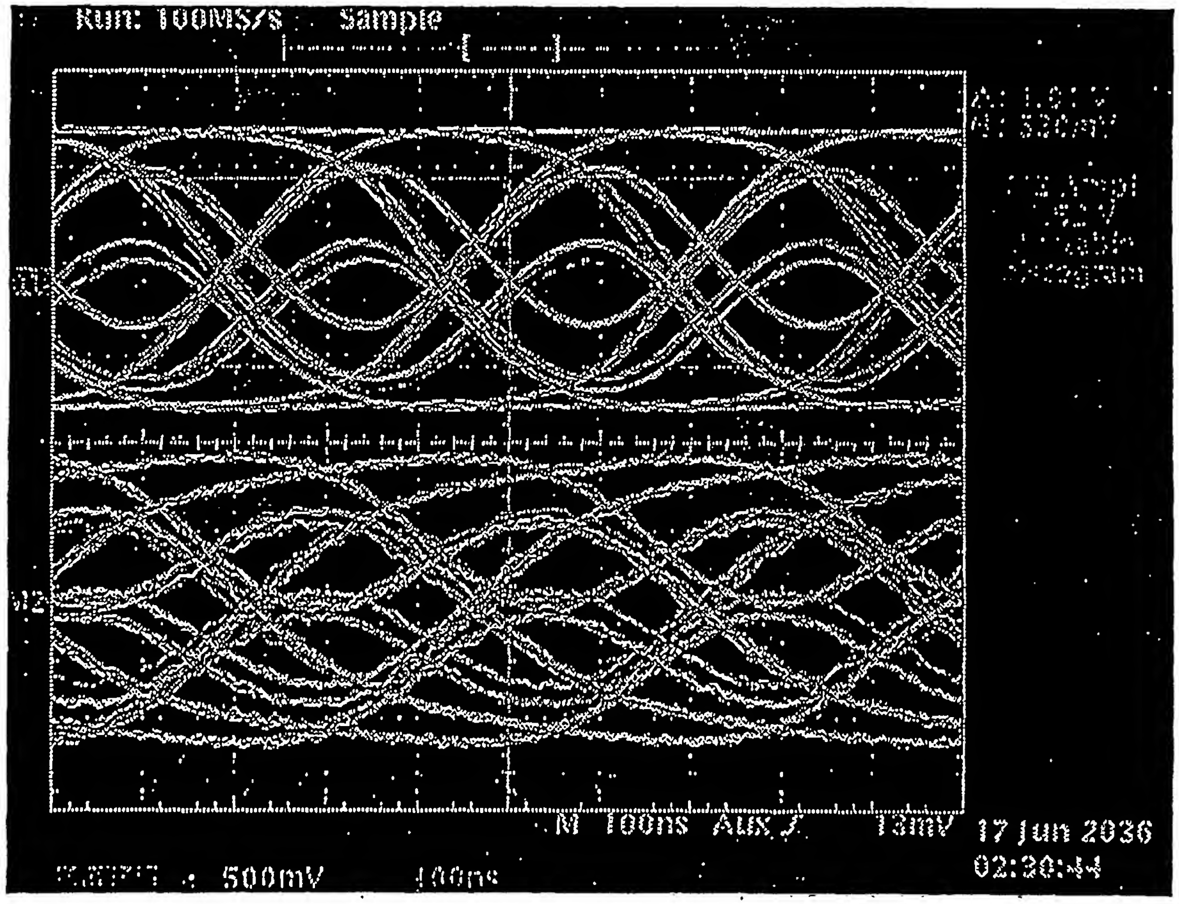


FIG. 11A

Firewire
25-feet IEEE 1394
No Equalization

FIG. 11B

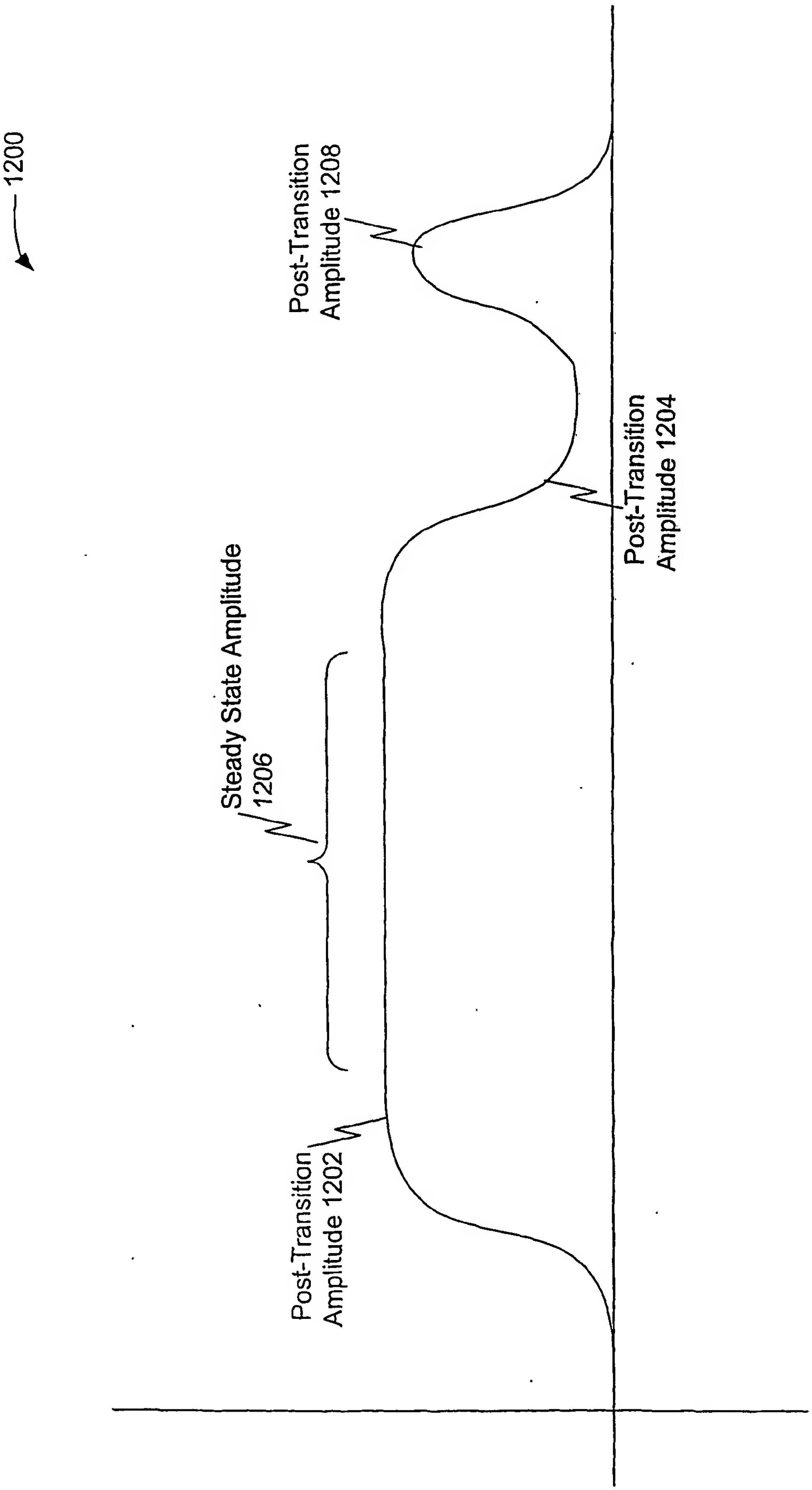
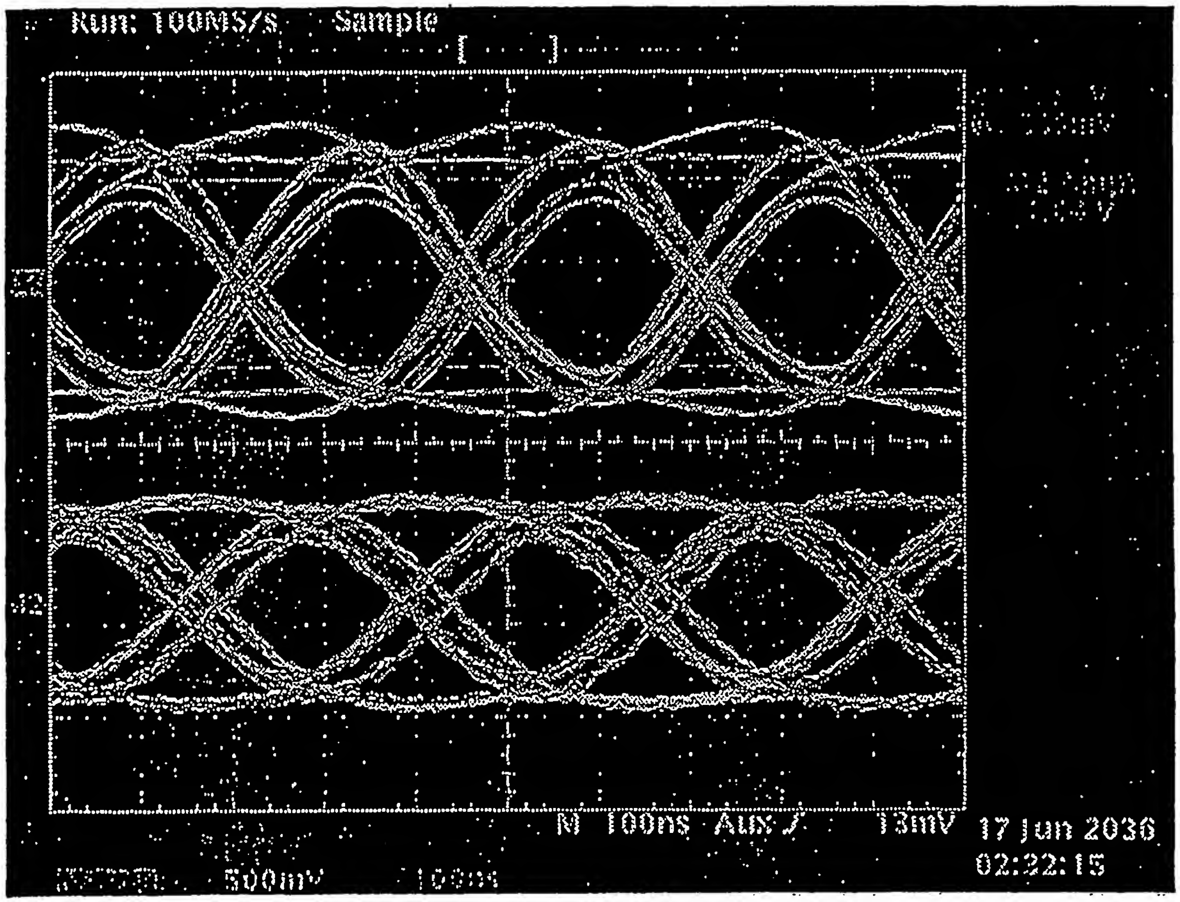

1200
Post-Transition Amplitude 1208
Post-Transition Amplitude 1204
Steady State Amplitude 1206
Post-Transition Amplitude 1202

FIG. 12

Receiver Eye Diagrams: 3.125-Gb/s

Backplane
36-inches FR4
Equalization
a = 0.25
Eye Opening = 900mV

FIG 13A



Firewire
25-feet IEEE 1394
Equalization
a = 0.375
Eye Opening = 750mV

FIG. 13B

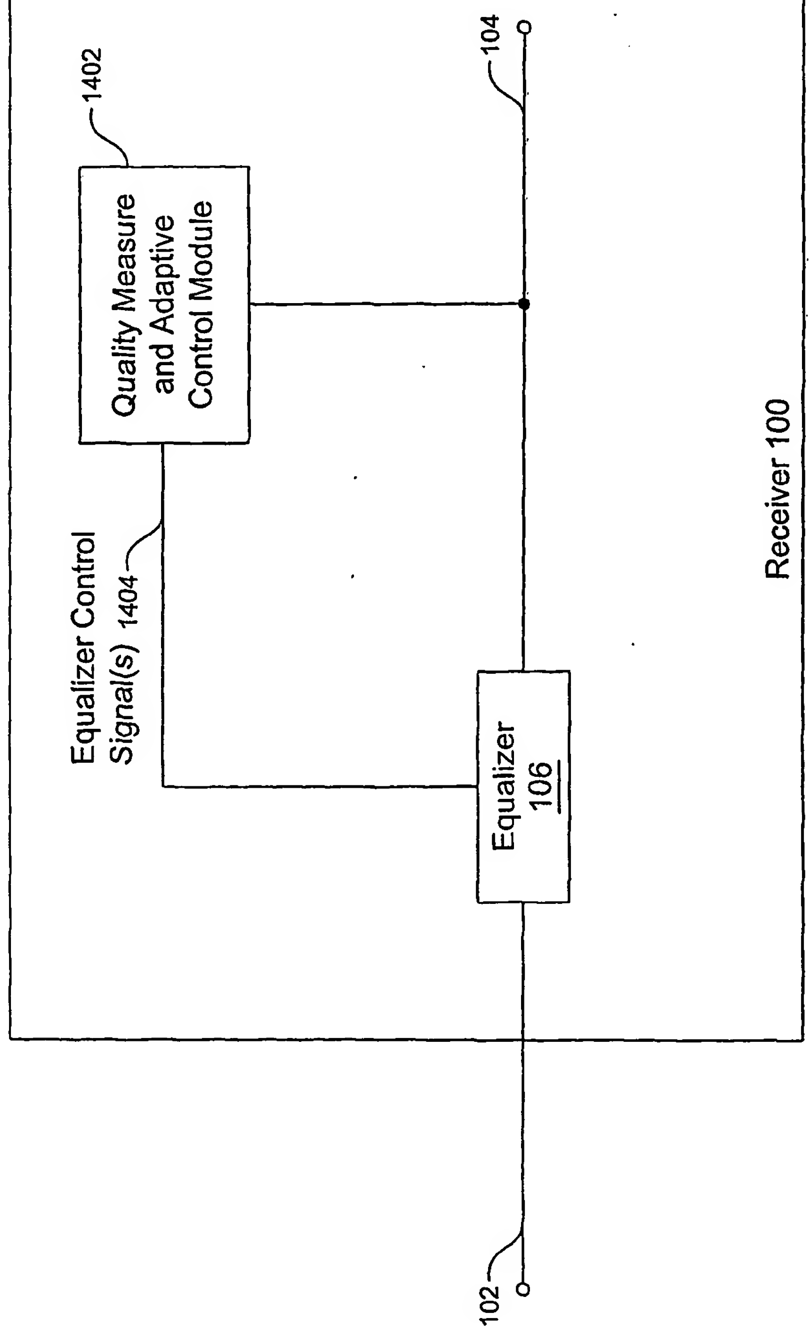

1402
Quality Measure and Adaptive Control Module
104
Equalizer Control Signal(s) 1404
Receiver 100
Equalizer 106
102

FIG. 14A

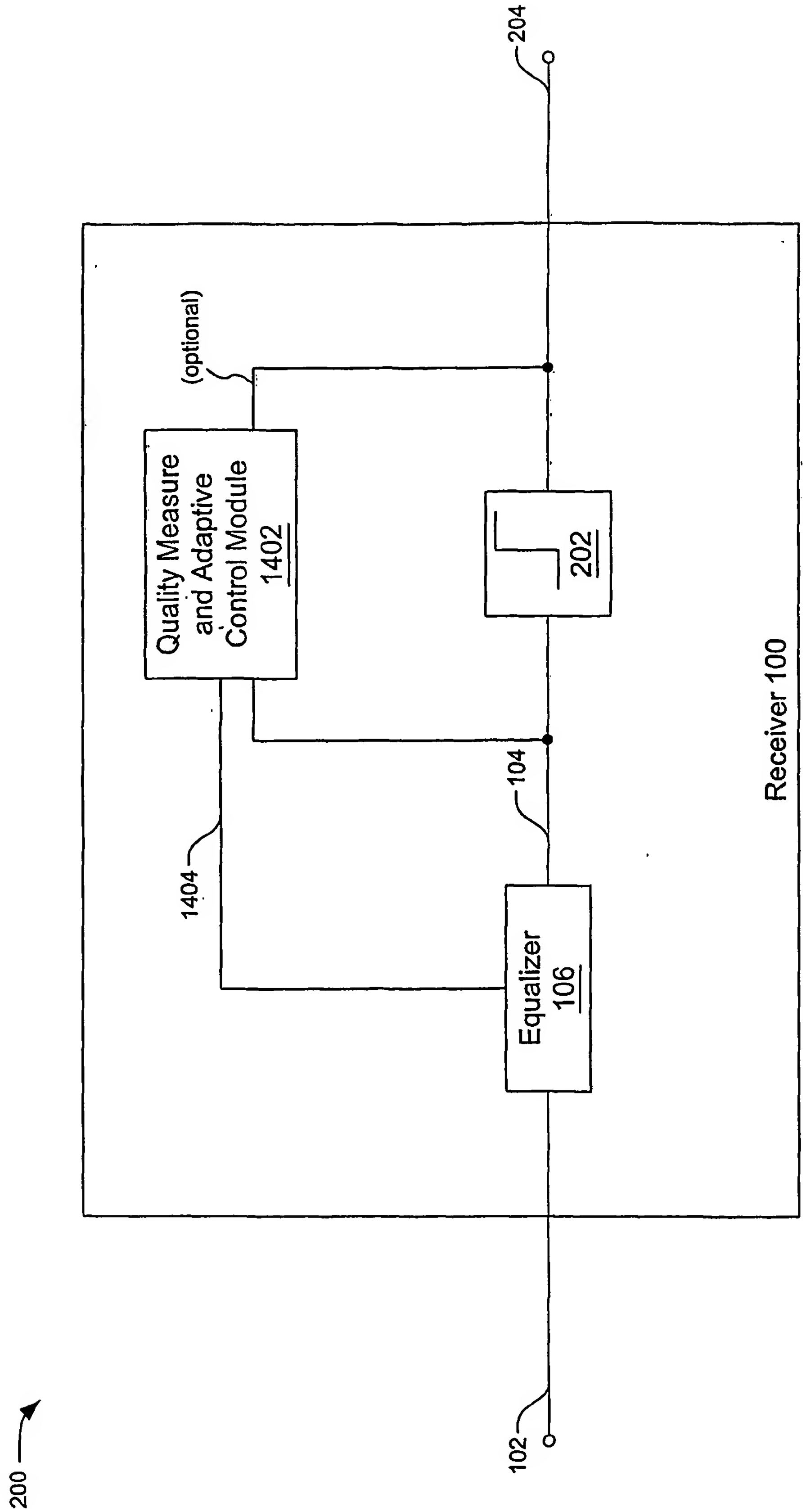

200
102
204
Receiver 100
Equalizer
106
104
202
Quality Measure
and Adaptive
Control Module
1402
1404
(optional)

FIG. 14B

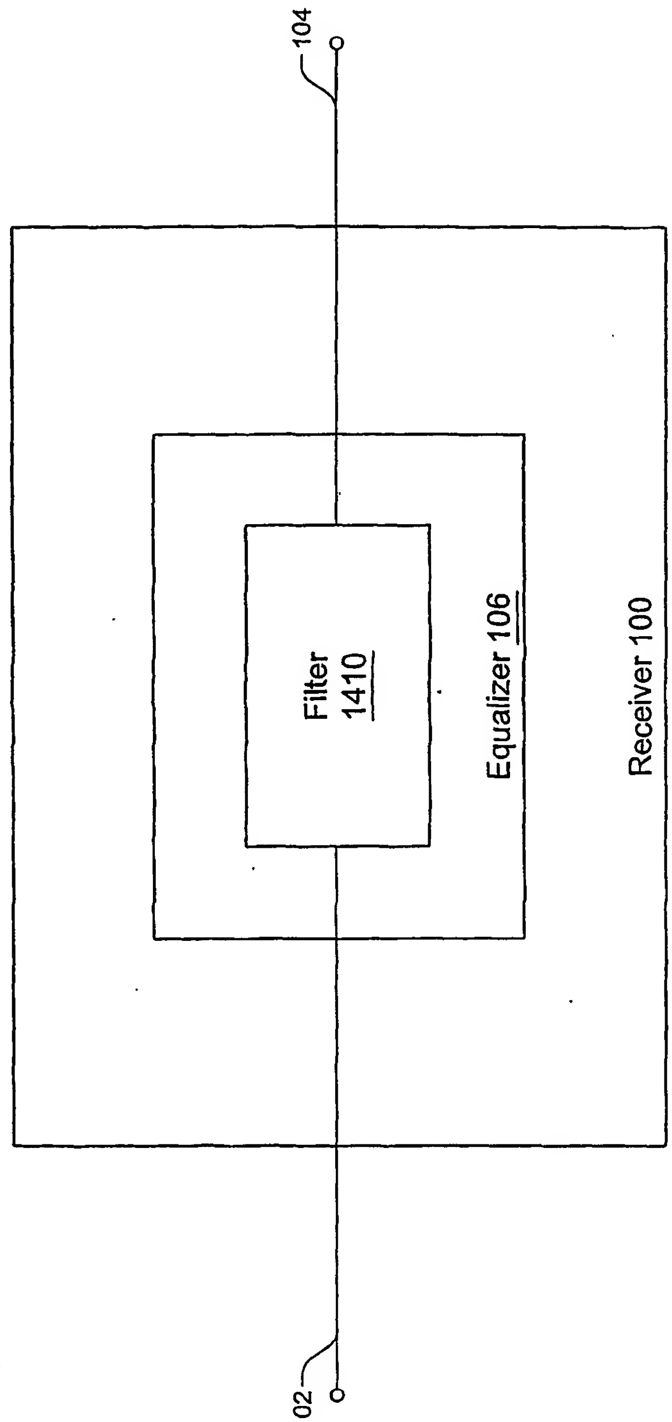


FIG. 14C

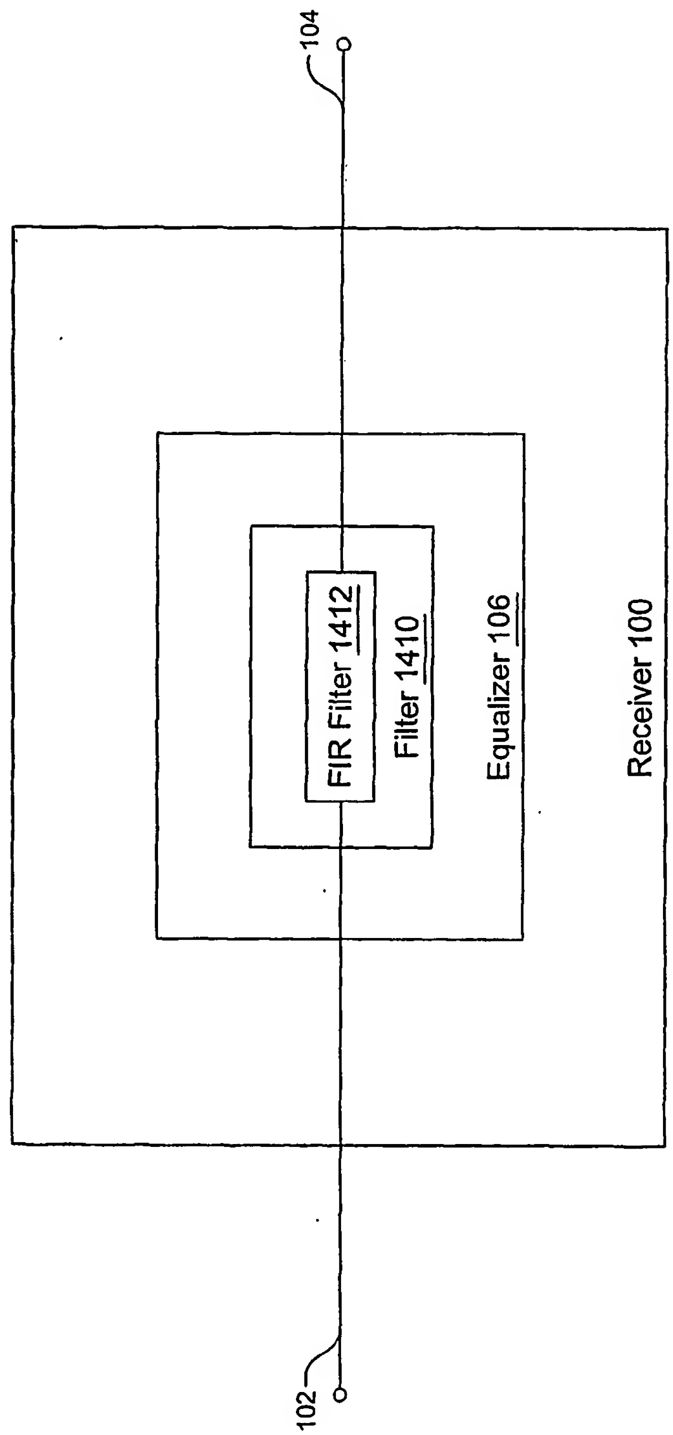

104
FIR Filter 1412
Filter 1410
Equalizer 106
Receiver 100
102

FIG. 14D

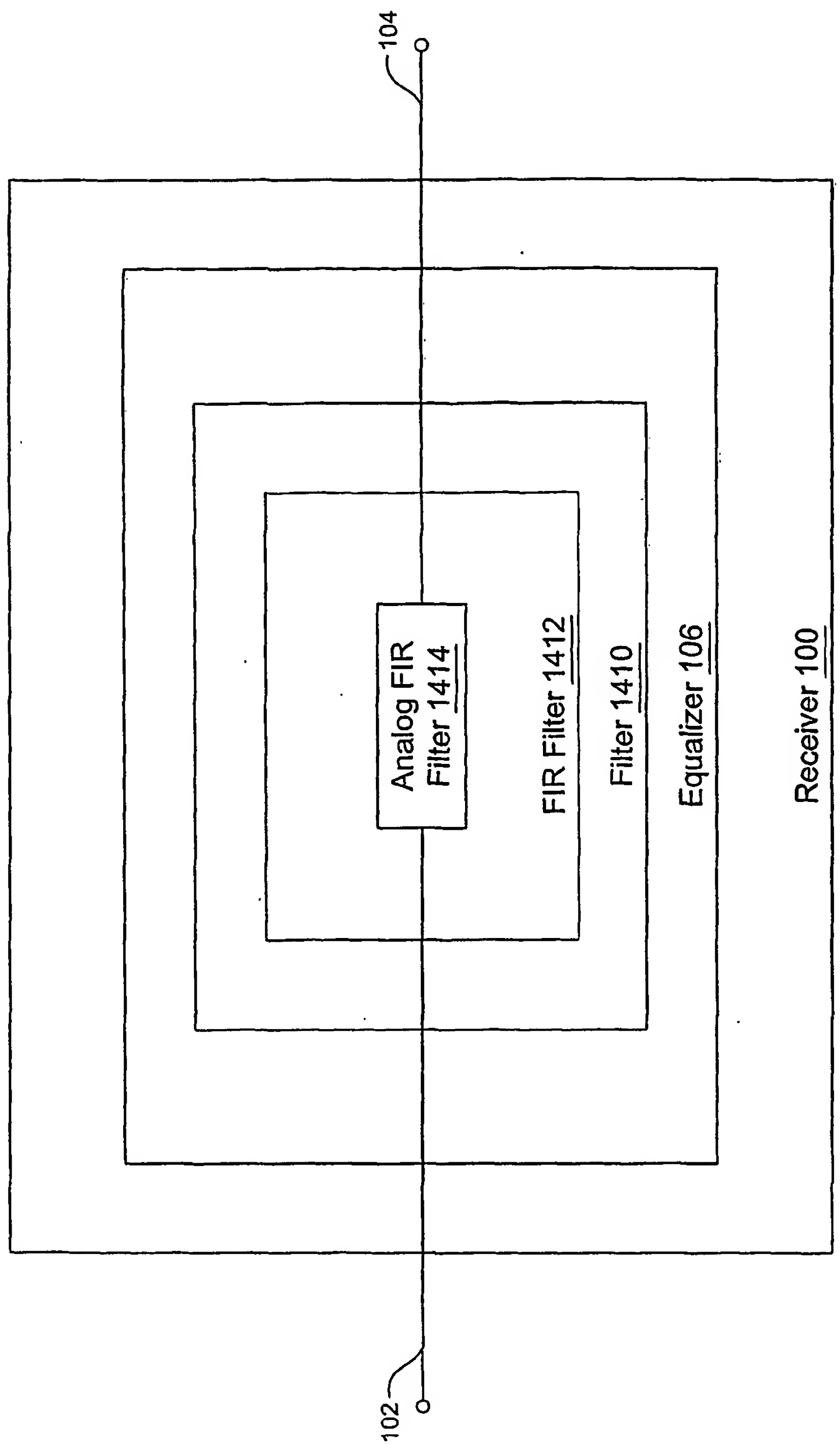

104
Analog FIR Filter 1414
FIR Filter 1412
Filter 1410
Equalizer 106
Receiver 100
102

FIG. 14E

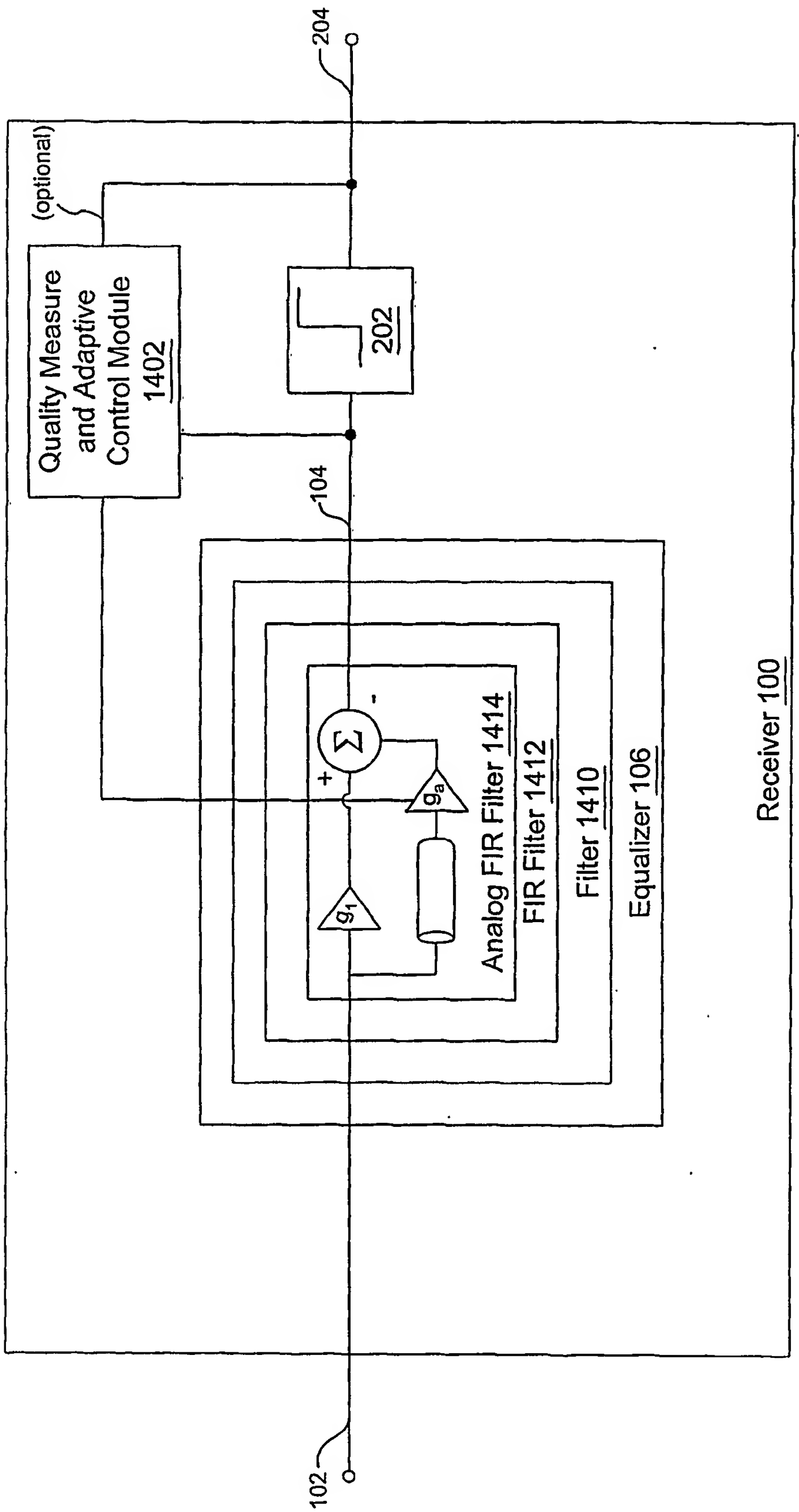

204
(optional)
Quality Measure and Adaptive Control Module 1402
202
104
+
-
Σ
g_a
g_1
Analog FIR Filter 1414
FIR Filter 1412
Filter 1410
Equalizer 106
Receiver 100
102

FIG. 14F

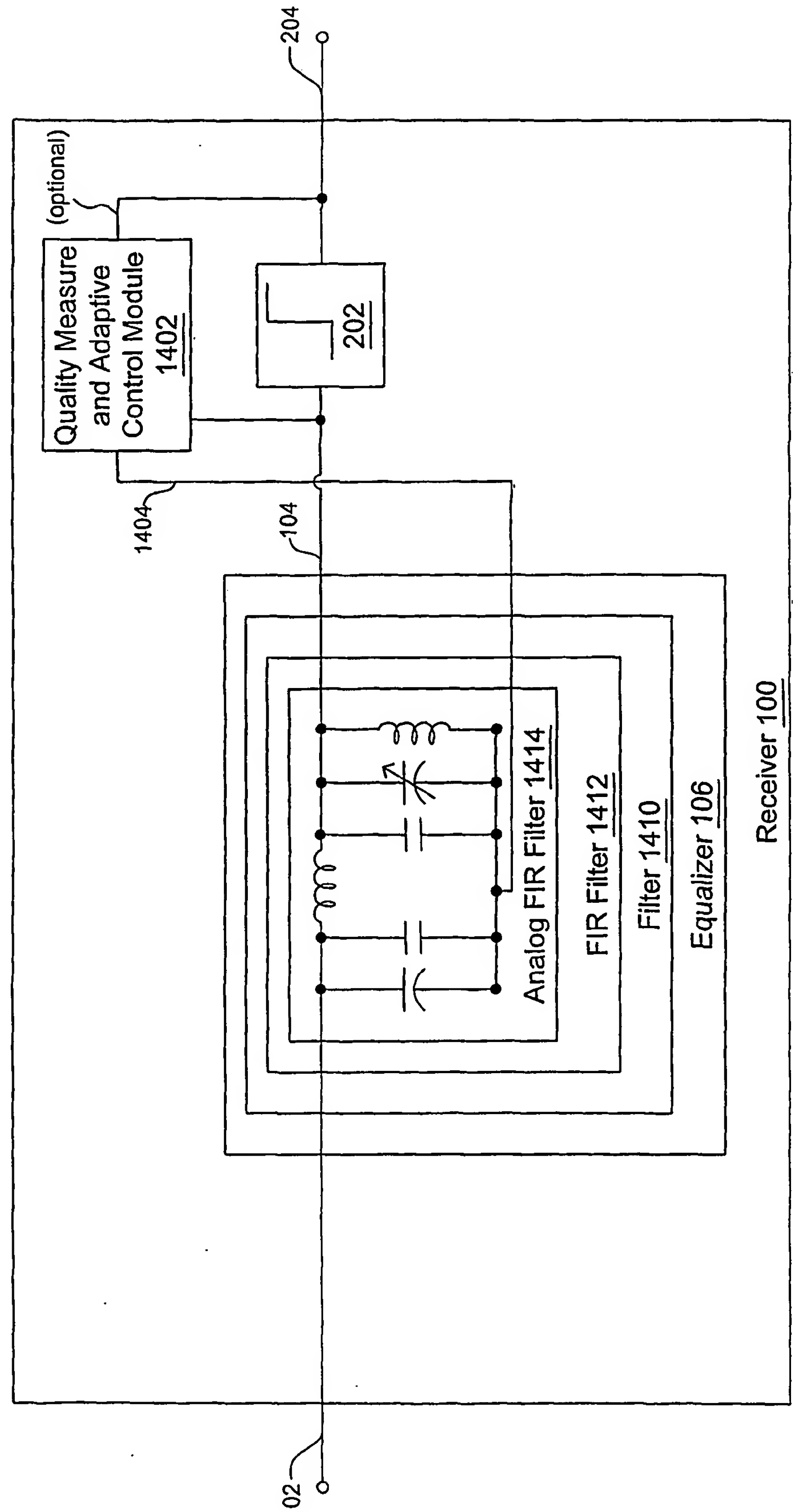

204
(optional)
Quality Measure and Adaptive Control Module 1402
202
1404
104
Analog FIR Filter 1414
FIR Filter 1412
Filter 1410
Equalizer 106
Receiver 100
102

FIG. 14G

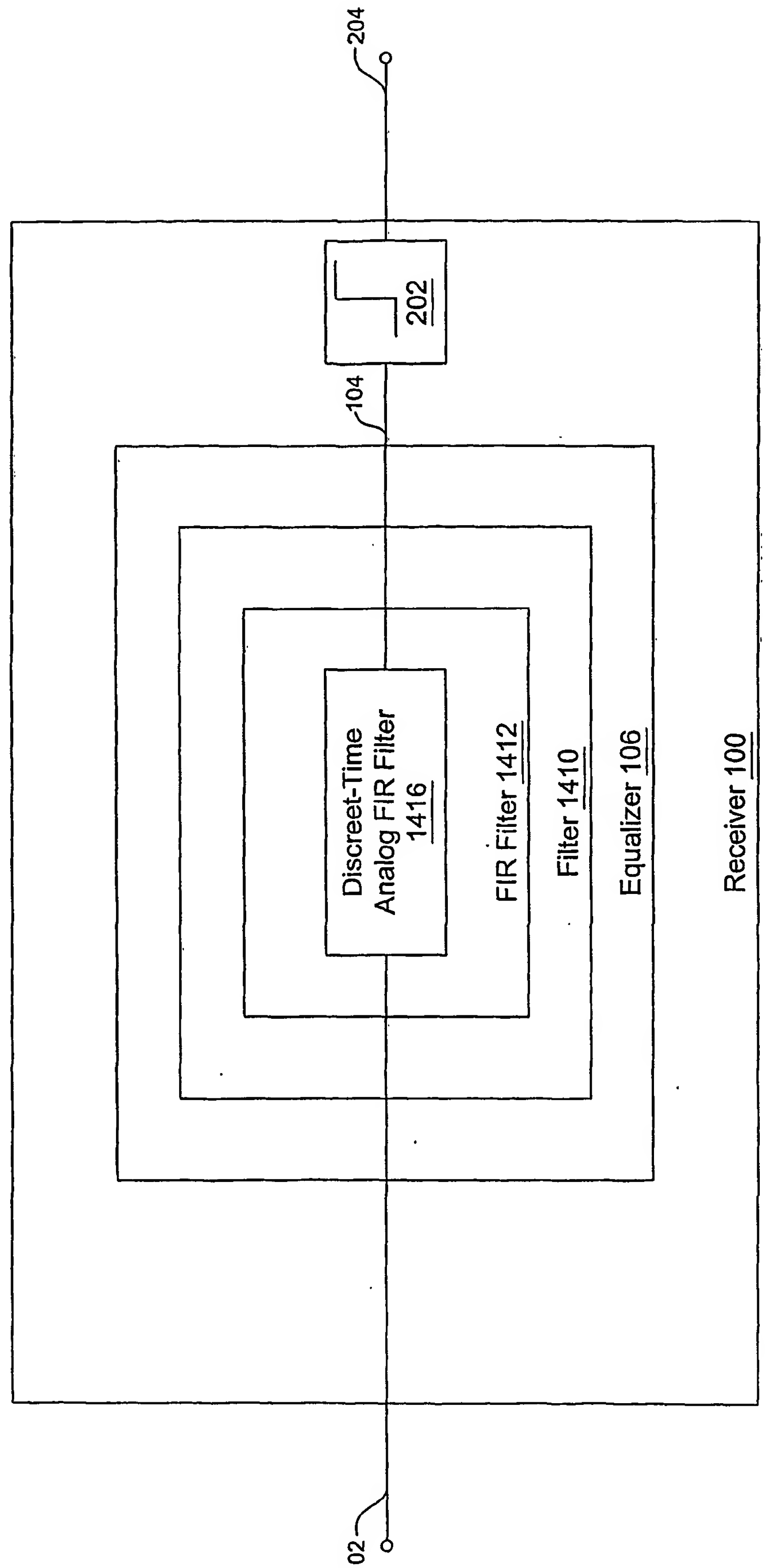

204
202
104
Discreet-Time
Analog FIR Filter
1416
FIR Filter 1412
Filter 1410
Equalizer 106
Receiver 100
102

FIG. 14H

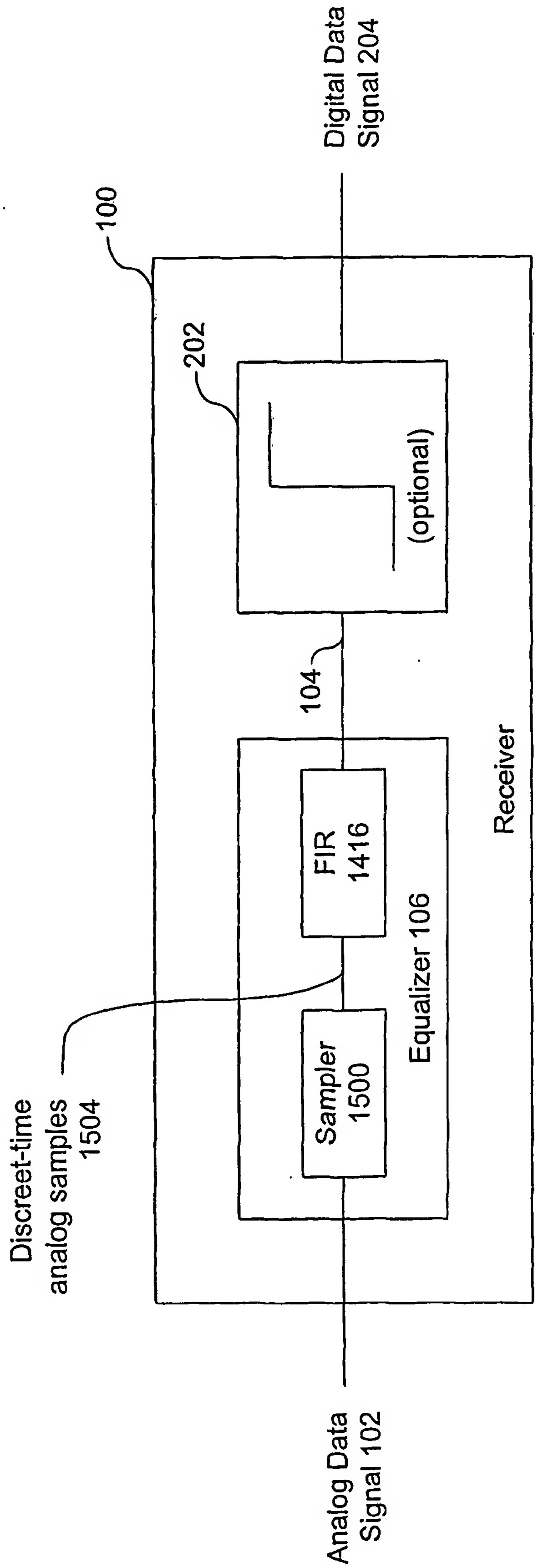

Digital Data
Signal 204
100
202
(optional)
104
Receiver
FIR
1416
Equalizer 106
Sampler
1500
Discreet-time
analog samples
1504
Analog Data
Signal 102

FIG. 15

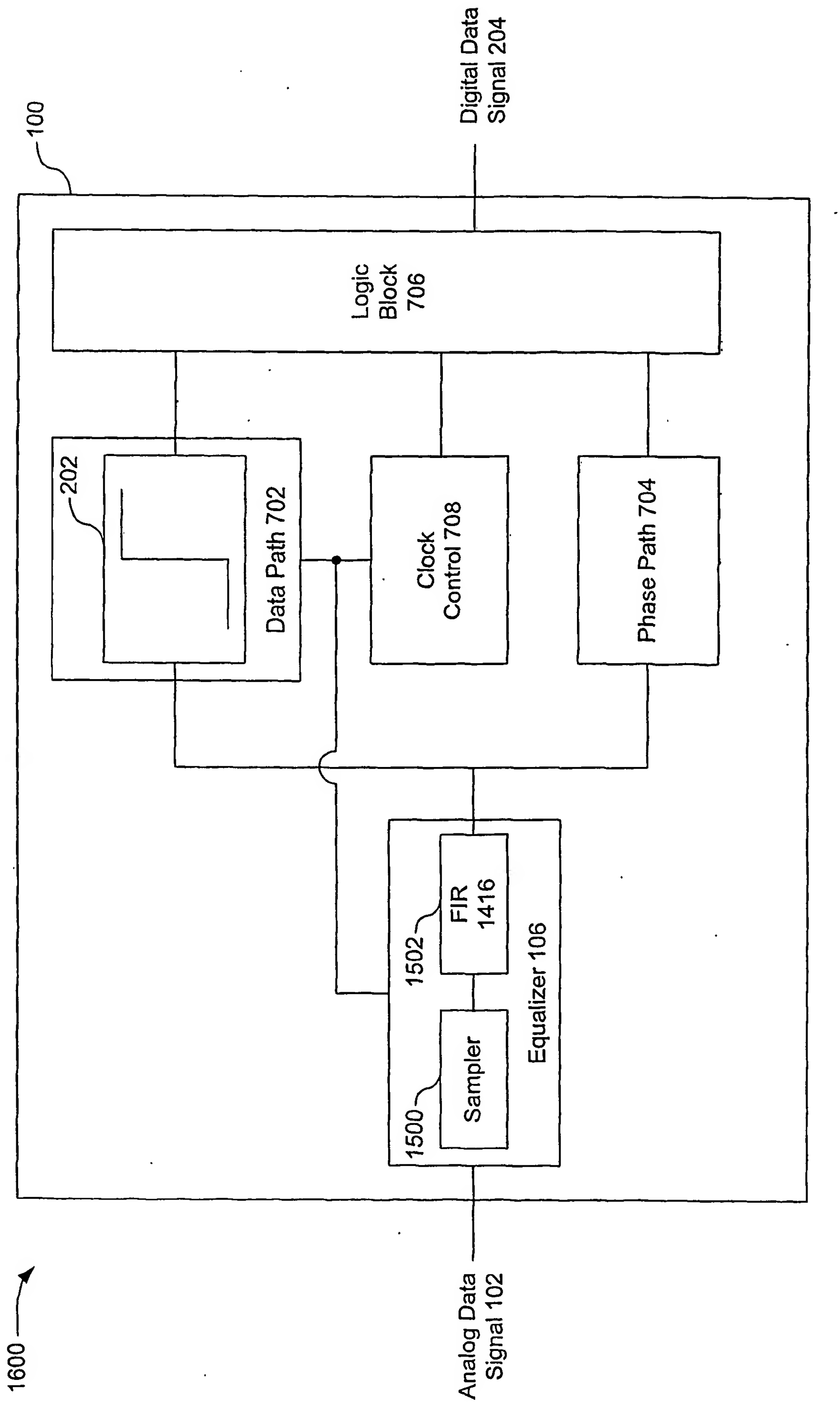

100
Digital Data Signal 204
Logic Block 706
202
Data Path 702
Clock Control 708
Phase Path 704
1502
FIR 1416
1500
Sampler
Equalizer 106
1600
Analog Data Signal 102

FIG. 16

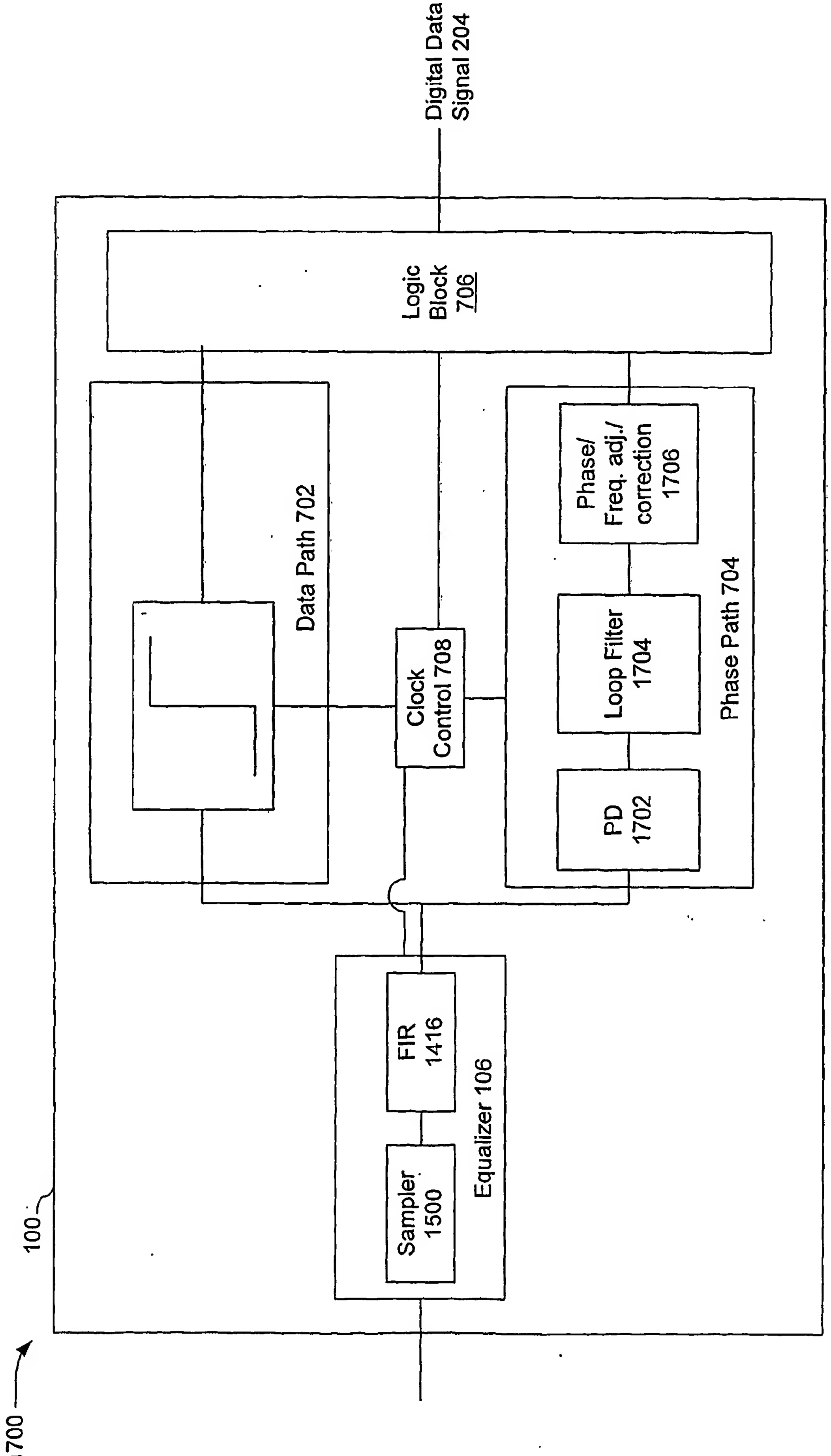

Digital Data Signal 204
Logic Block 706
Data Path 702
Clock Control 708
Phase/ Freq. adj./ correction 1706
Loop Filter 1704
PD 1702
Phase Path 704
FIR 1416
Sampler 1500
Equalizer 106
100
1700

FIG. 17

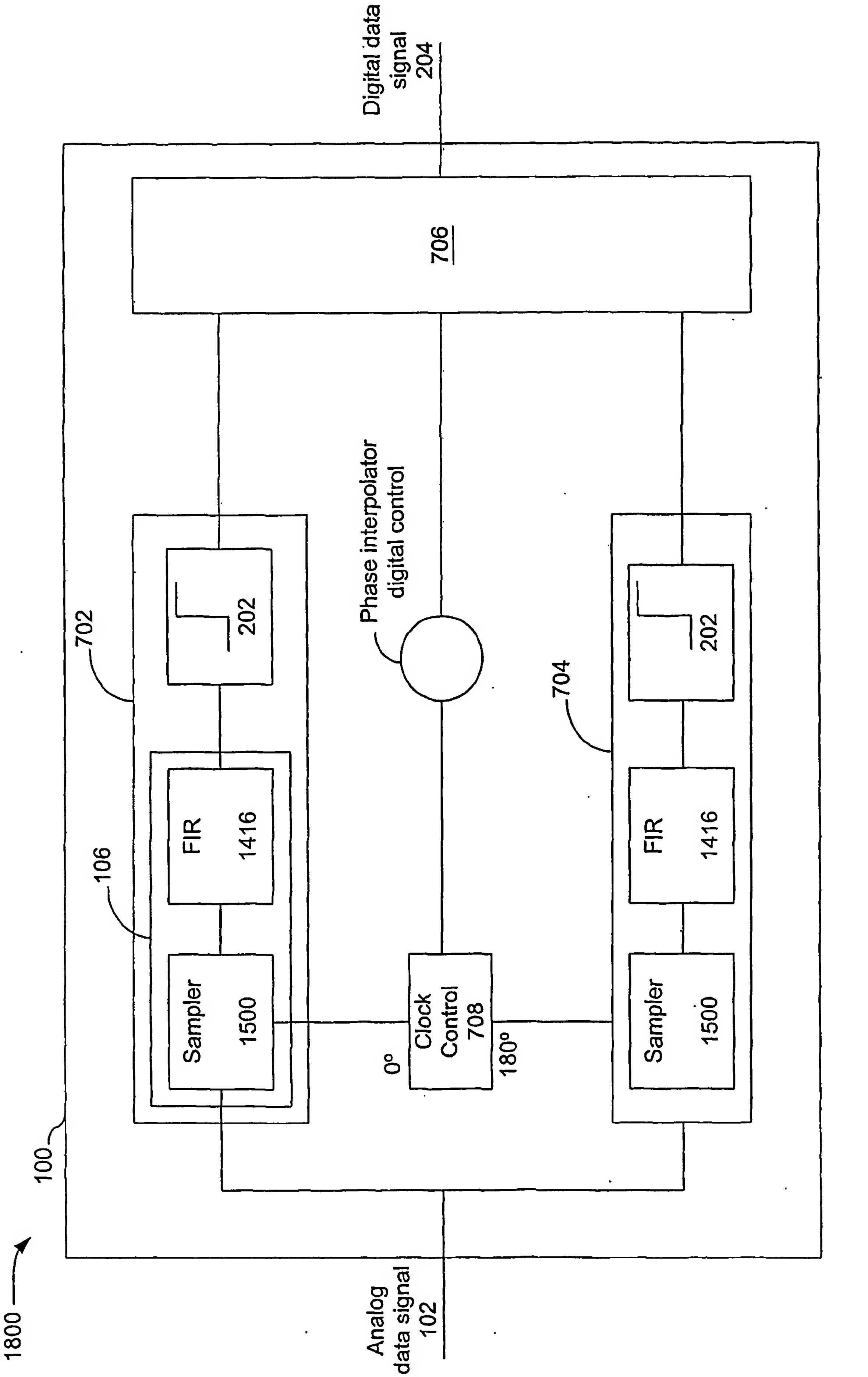

Digital data signal 204
706
702
202
106
FIR
1416
Sampler
1500
Phase interpolator digital control
Clock Control 708
0°
180°
704
202
FIR
1416
Sampler
1500
100
1800
Analog data signal 102

FIG. 18

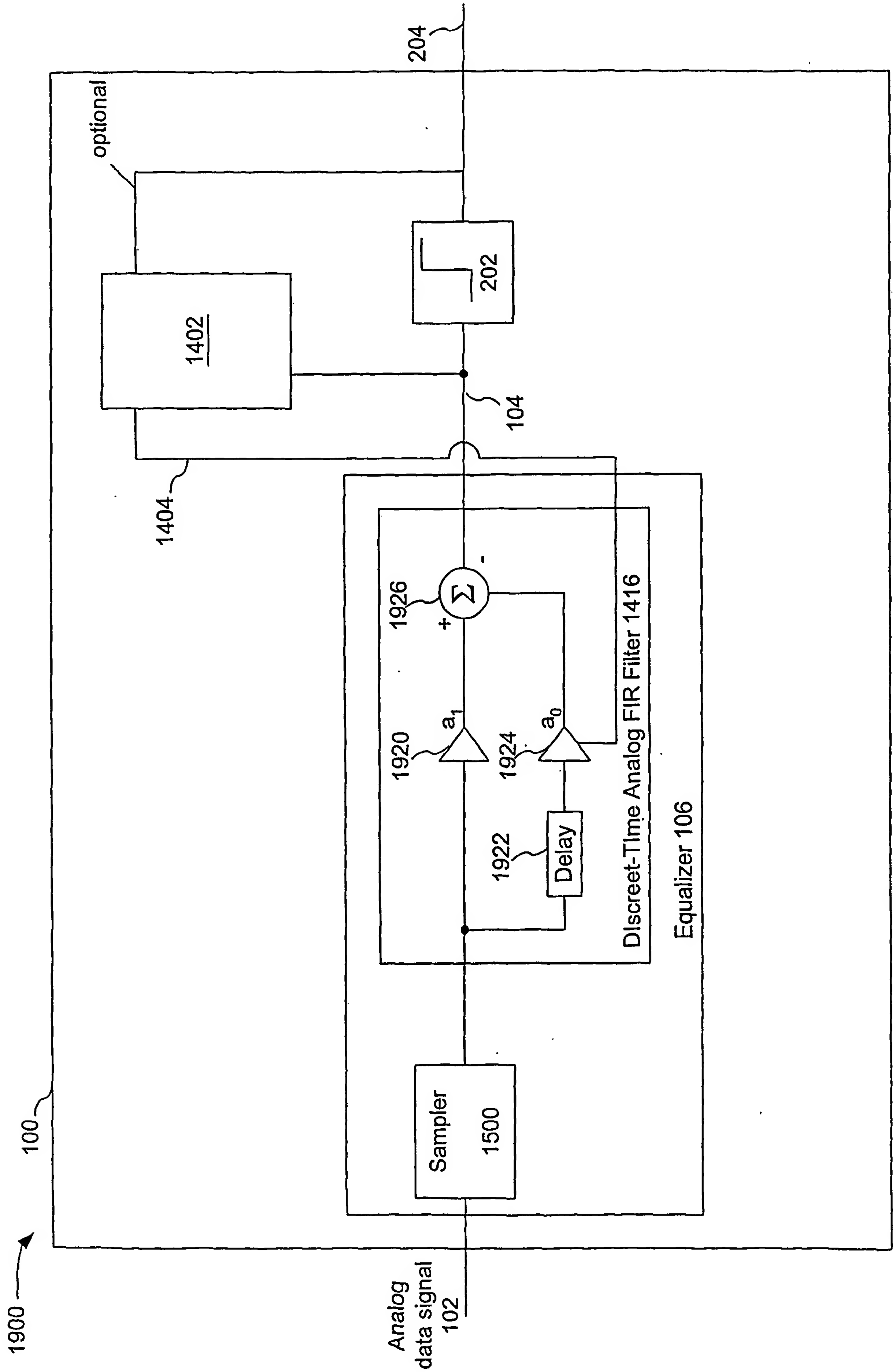

204
optional
1402
202
104
1404
1926
Σ
+
-
a1
a0
1920
1924
1922
Delay
Discreet-Time Analog FIR Filter 1416
Equalizer 106
100
Sampler
1500
1900
Analog data signal 102

FIG. 19

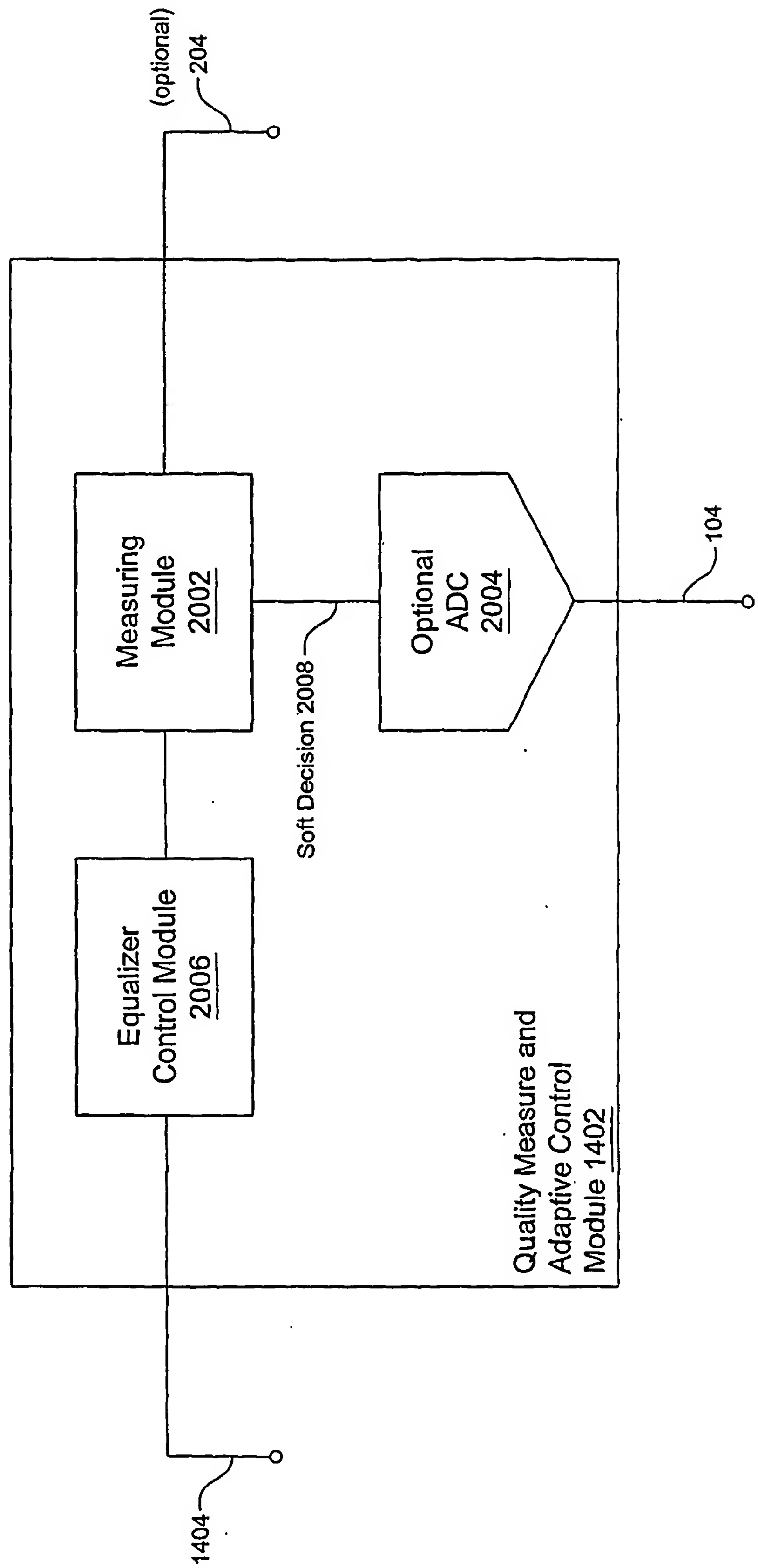

(optional)
204
Measuring
Module
2002
Optional
ADC
2004
104
Soft Decision 2008
Equalizer
Control Module
2006
Quality Measure and
Adaptive Control
Module 1402
1404

FIG. 20

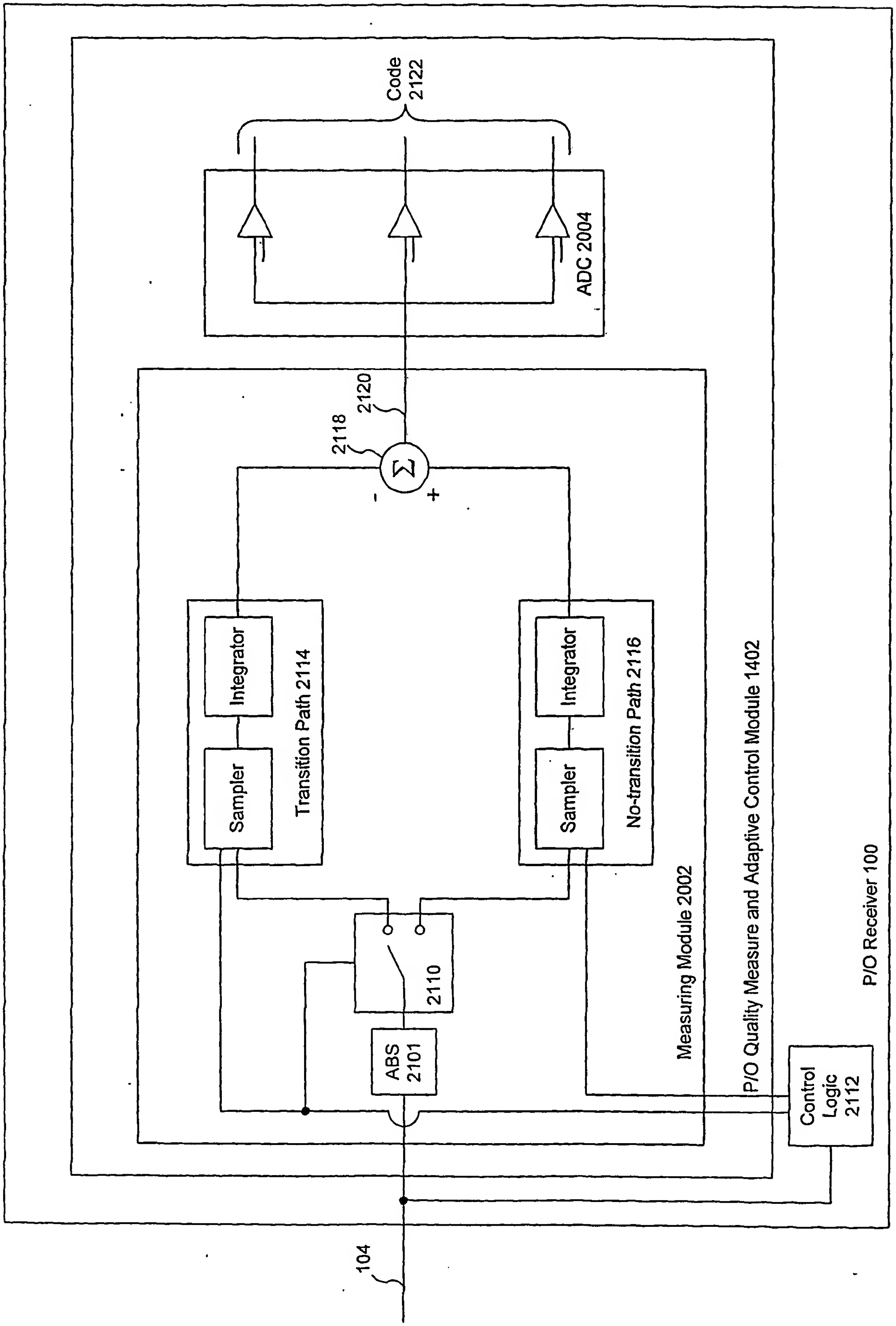

Code
2122
ADC 2004
2120
2118
Σ
-
+
Integrator
Sampler
Transition Path 2114
Integrator
Sampler
No-transition Path 2116
2110
ABS
2101
Measuring Module 2002
P/O Quality Measure and Adaptive Control Module 1402
Control
Logic
2112
P/O Receiver 100
104

FIG. 21A

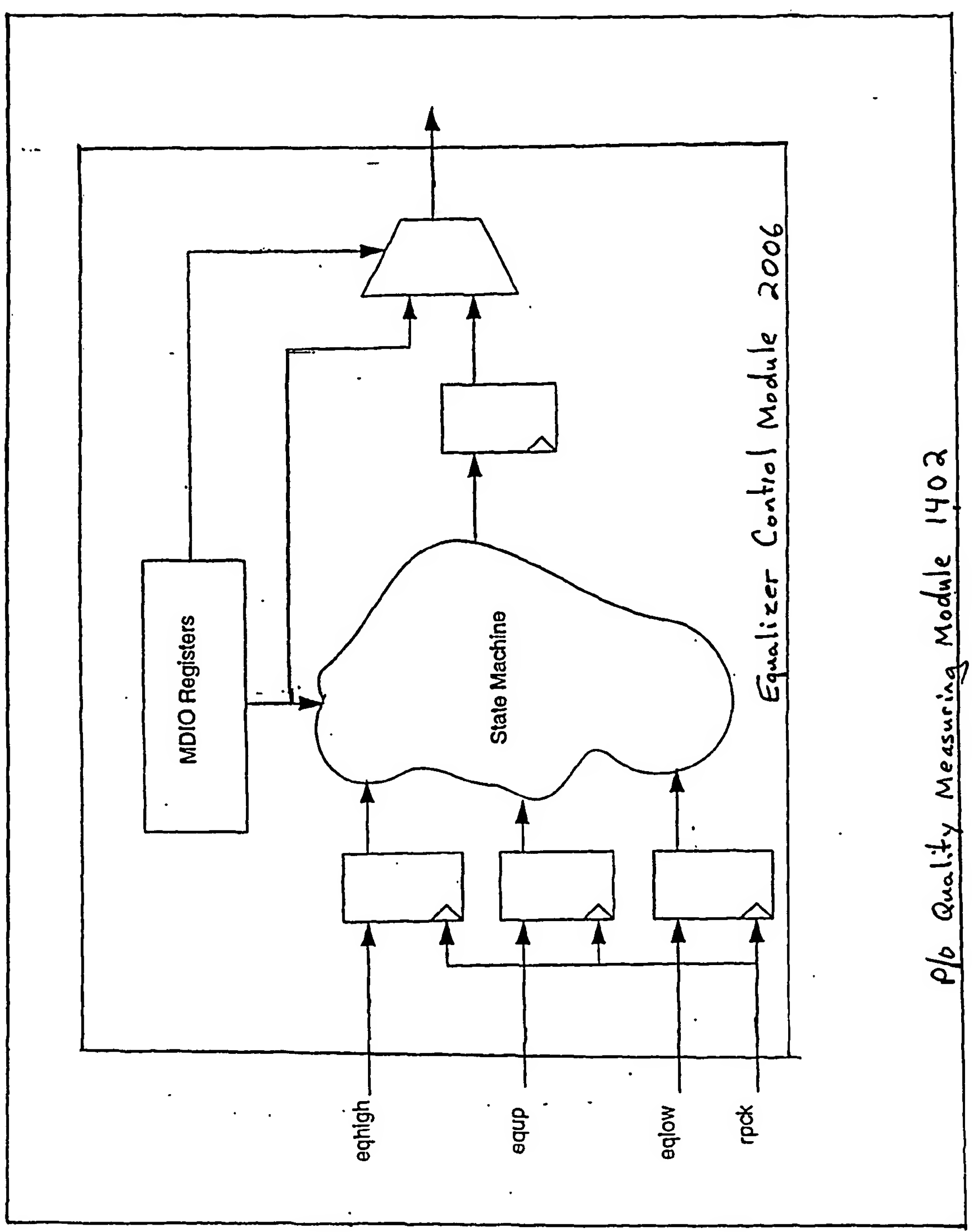

MDIO Registers
State Machine
eqhigh
equp
eqlow
rpck
Equalizer Control Module 2006
P/O Quality Measuring Module 1402

FIG. 21B

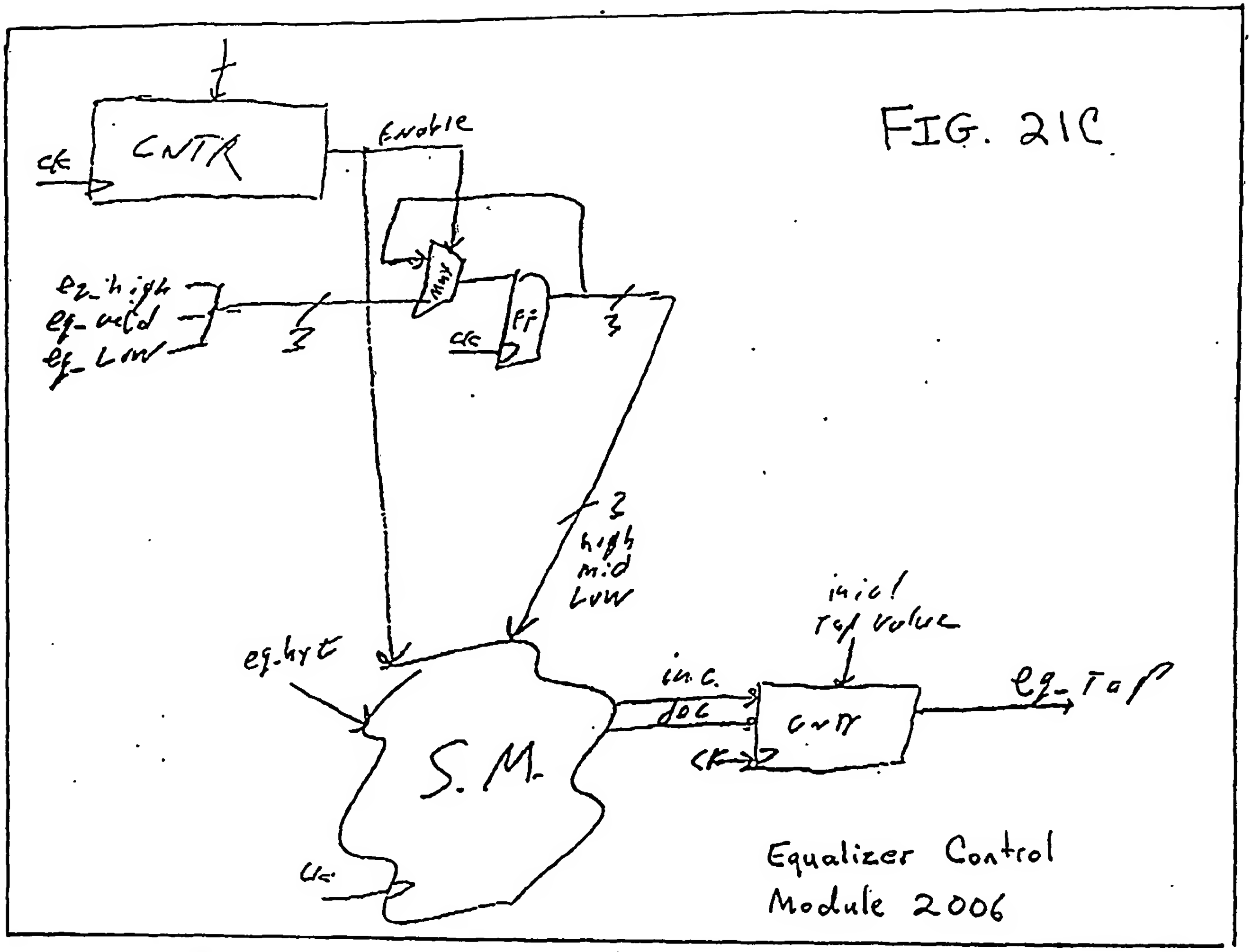


FIG. 21C

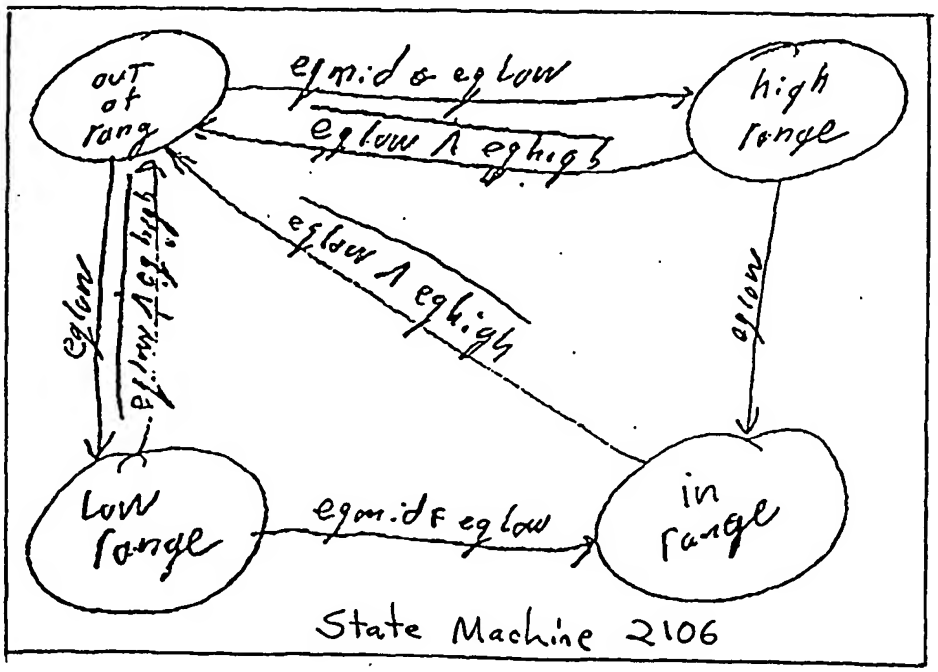


FIG. 21D

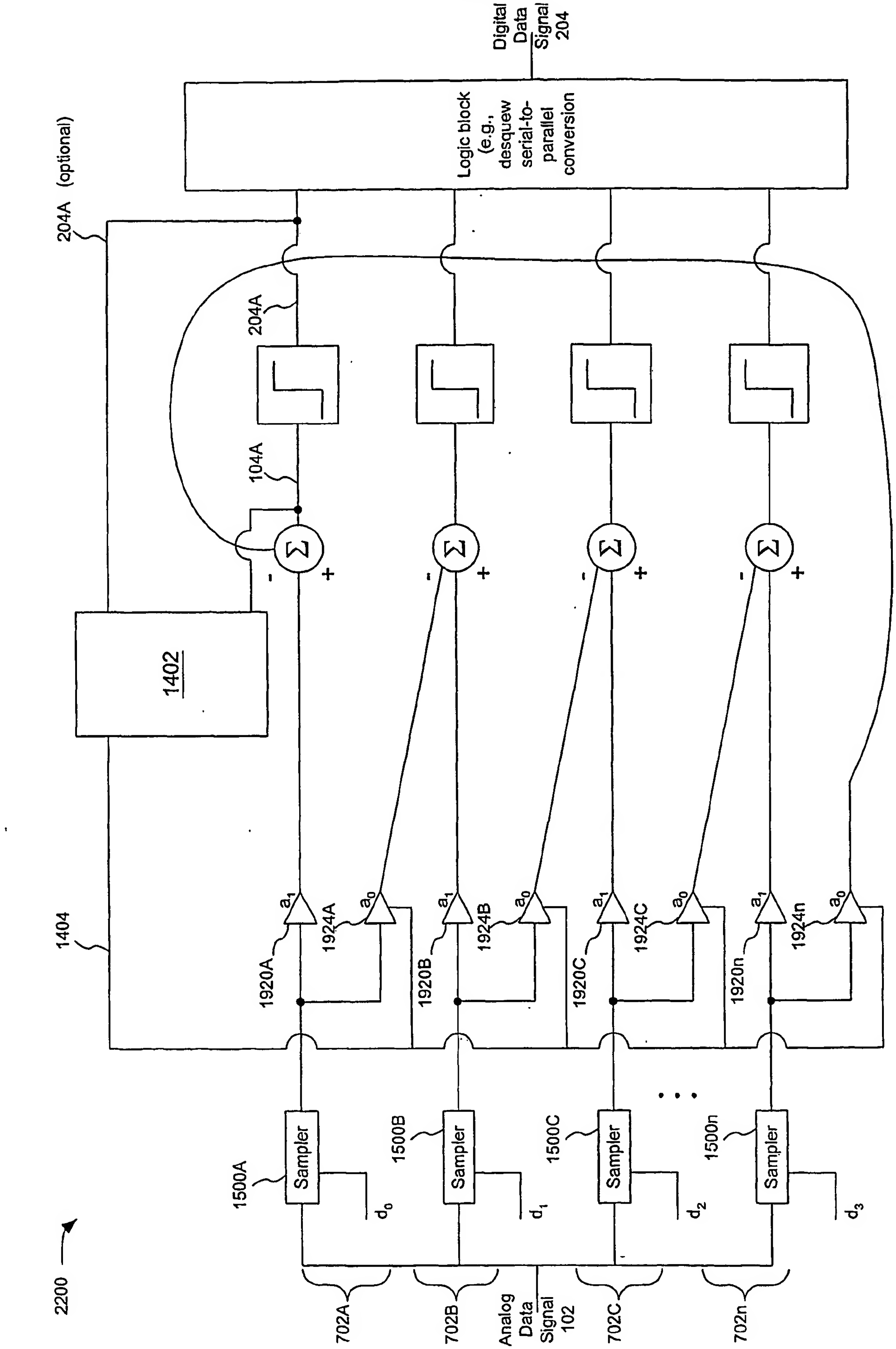

Digital Data Signal 204
Logic block (e.g., desquew serial-to-parallel conversion
204A (optional)
204A
104A
1402
1404
1920A
1924A
1920B
1924B
1920C
1924C
1920n
1924n
a_1
a_0
Σ
-
+
1500A
1500B
1500C
1500n
Sampler
d_0
d_1
d_2
d_3
2200
702A
702B
Analog Data Signal 102
702C
702n

FIG. 22

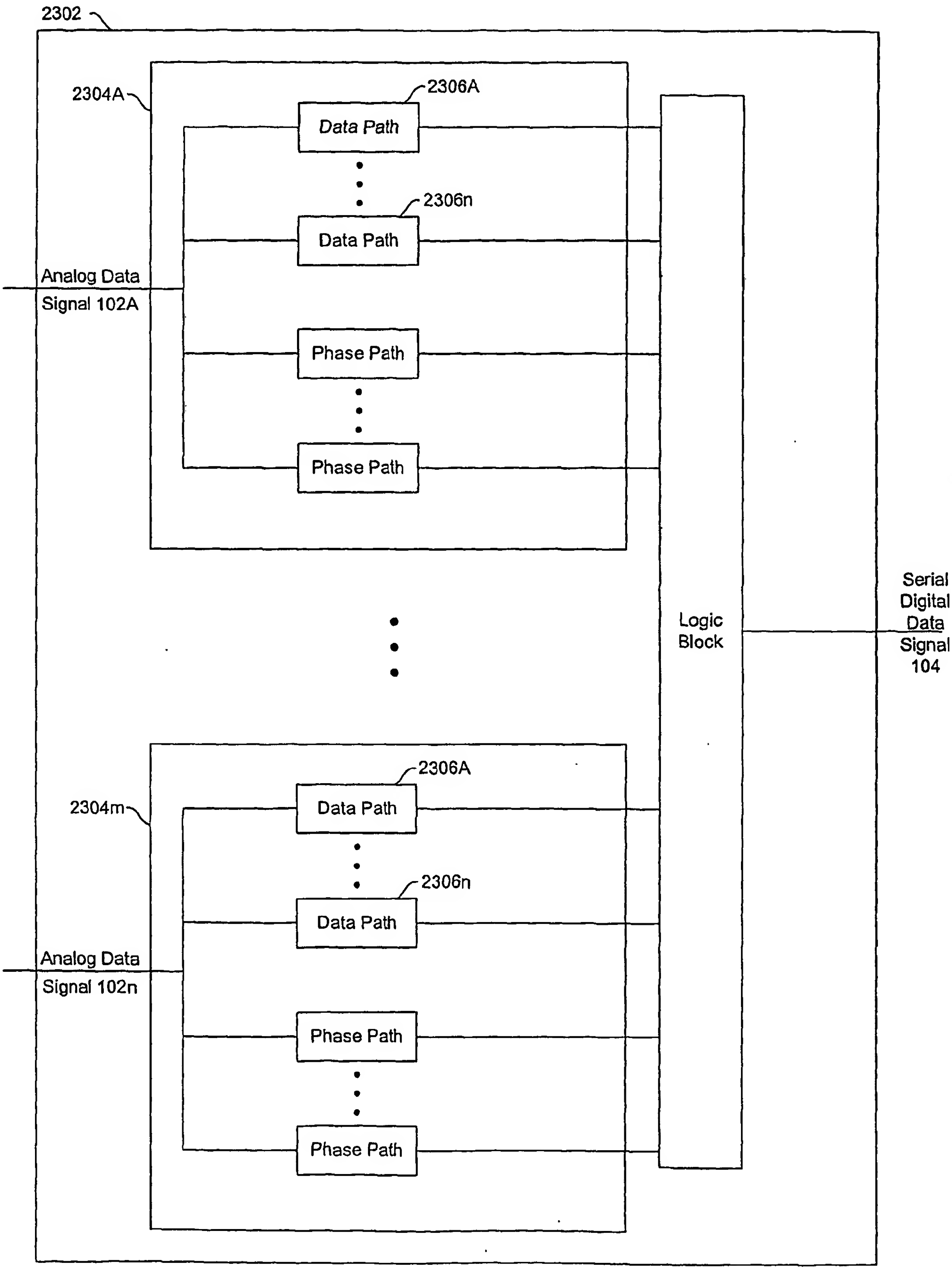

2302
2304A
2306A
Data Path
2306n
Data Path
Analog Data
Signal 102A
Phase Path
Phase Path
Logic
Block
Serial
Digital
Data
Signal
104
2304m
2306A
Data Path
2306n
Data Path
Analog Data
Signal 102n
Phase Path
Phase Path

FIG. 23

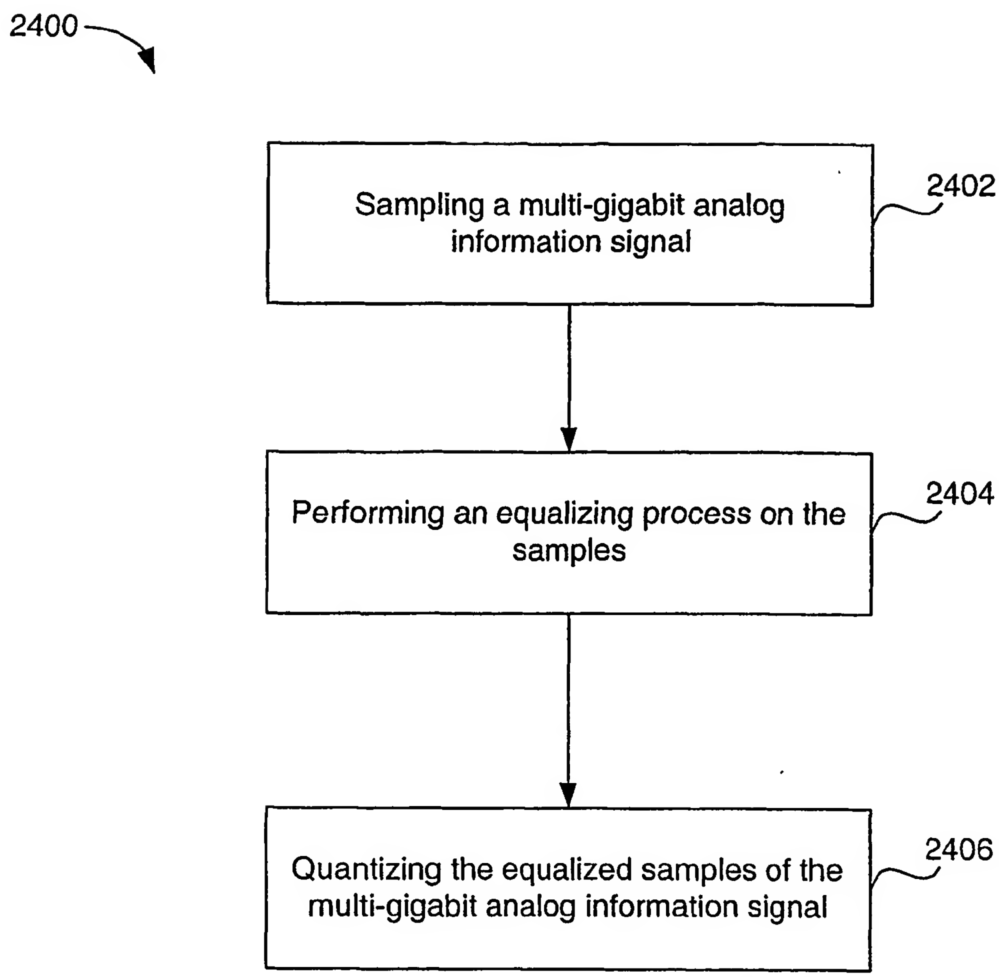

2400
Sampling a multi-gigabit analog information signal
2402
Performing an equalizing process on the samples
2404
Quantizing the equalized samples of the multi-gigabit analog information signal
2406

FIG. 24

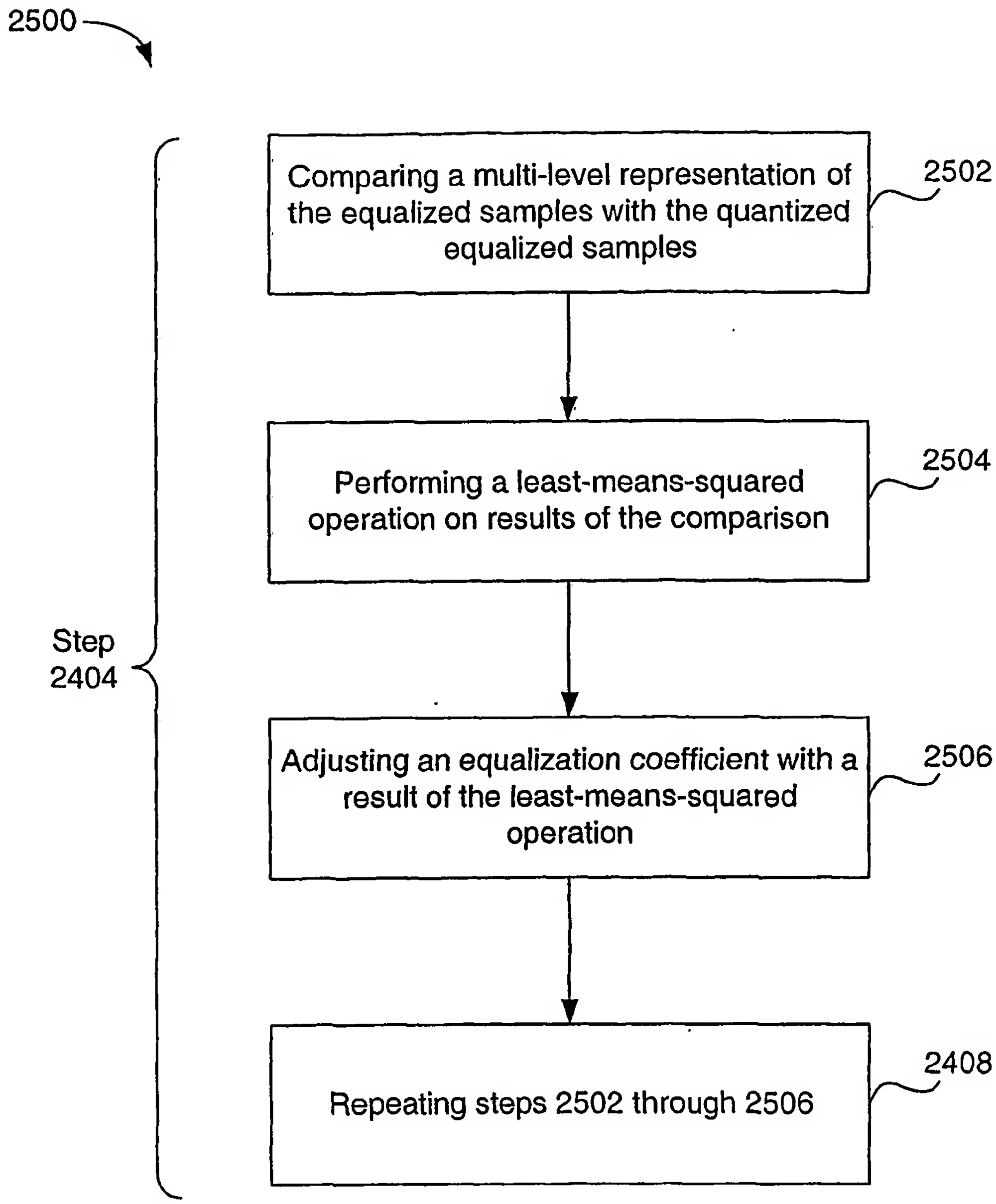

2500
Comparing a multi-level representation of the equalized samples with the quantized equalized samples
2502
Performing a least-means-squared operation on results of the comparison
2504
Adjusting an equalization coefficient with a result of the least-means-squared operation
2506
Repeating steps 2502 through 2506
2408
Step 2404

FIG. 25

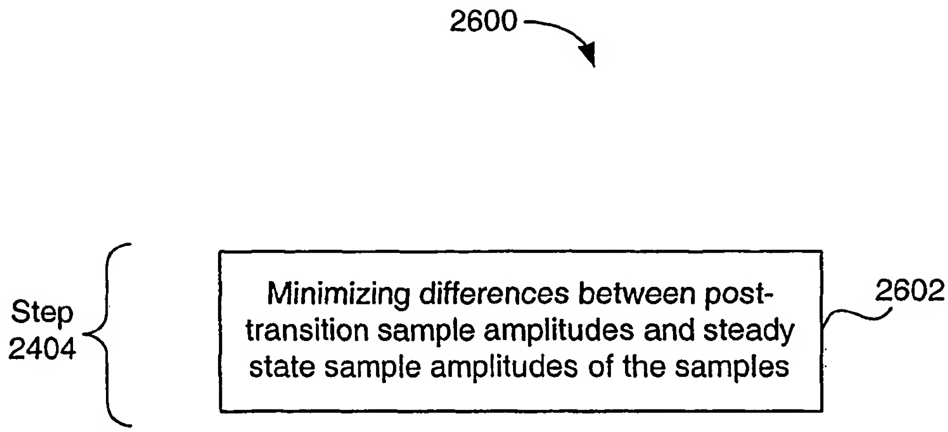

2600
Step 2404
Minimizing differences between post-transition sample amplitudes and steady state sample amplitudes of the samples
2602

FIG. 26

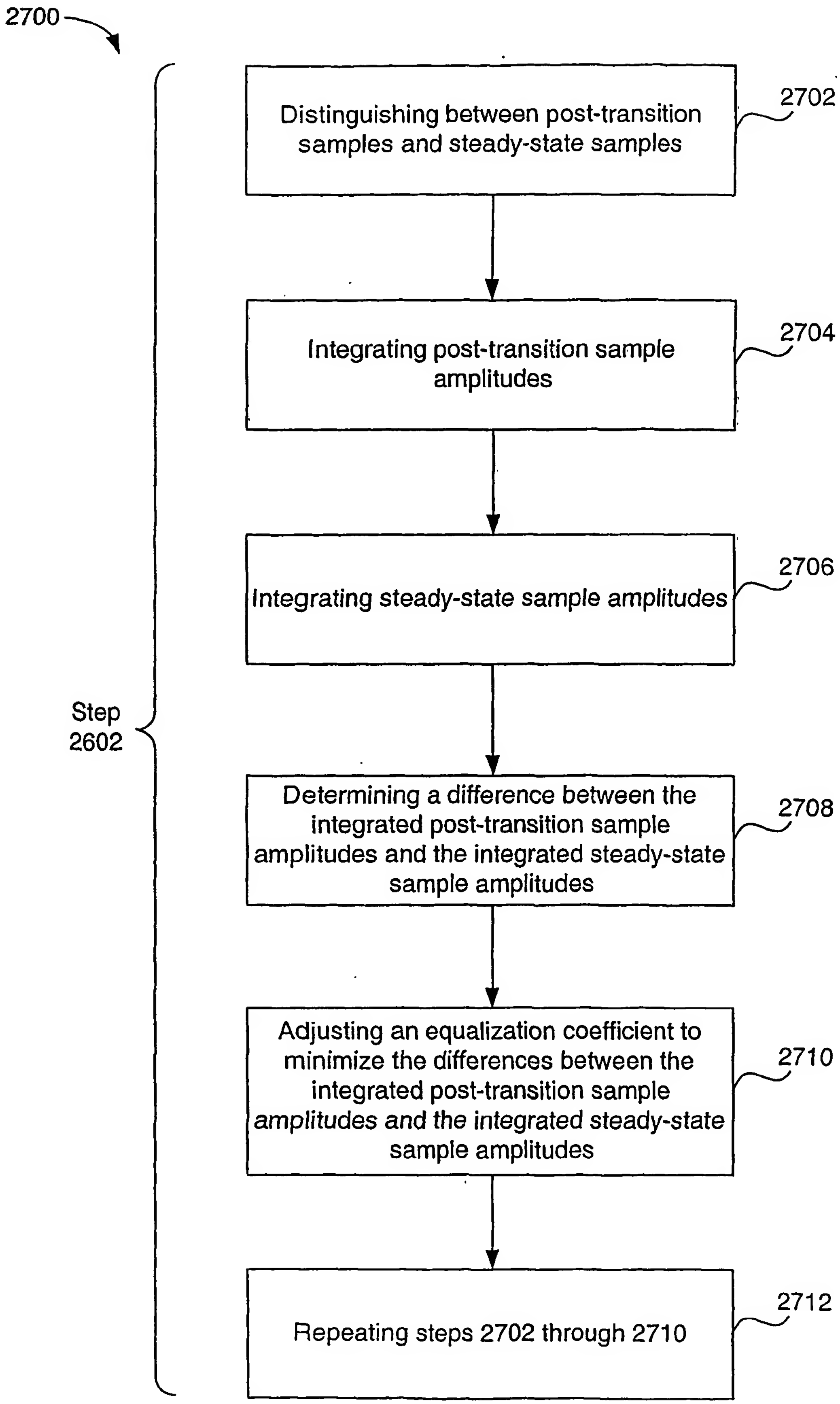

2700
Distinguishing between post-transition samples and steady-state samples
2702
Integrating post-transition sample amplitudes
2704
Integrating steady-state sample amplitudes
2706
Determining a difference between the integrated post-transition sample amplitudes and the integrated steady-state sample amplitudes
2708
Adjusting an equalization coefficient to minimize the differences between the integrated post-transition sample amplitudes and the integrated steady-state sample amplitudes
2710
Repeating steps 2702 through 2710
2712
Step 2602

FIG. 27

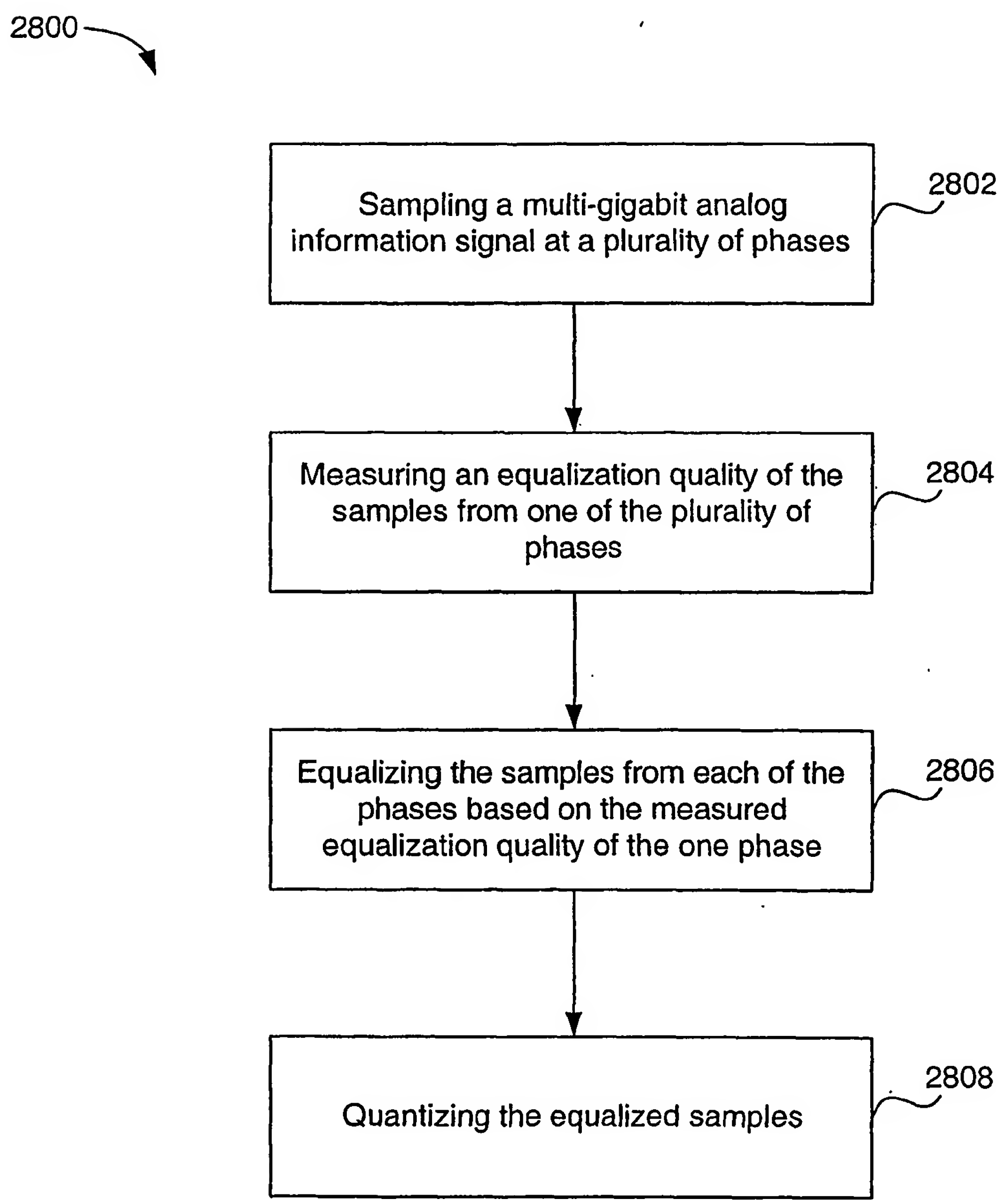

2800
Sampling a multi-gigabit analog information signal at a plurality of phases
2802
Measuring an equalization quality of the samples from one of the plurality of phases
2804
Equalizing the samples from each of the phases based on the measured equalization quality of the one phase
2806
Quantizing the equalized samples
2808

FIG. 28

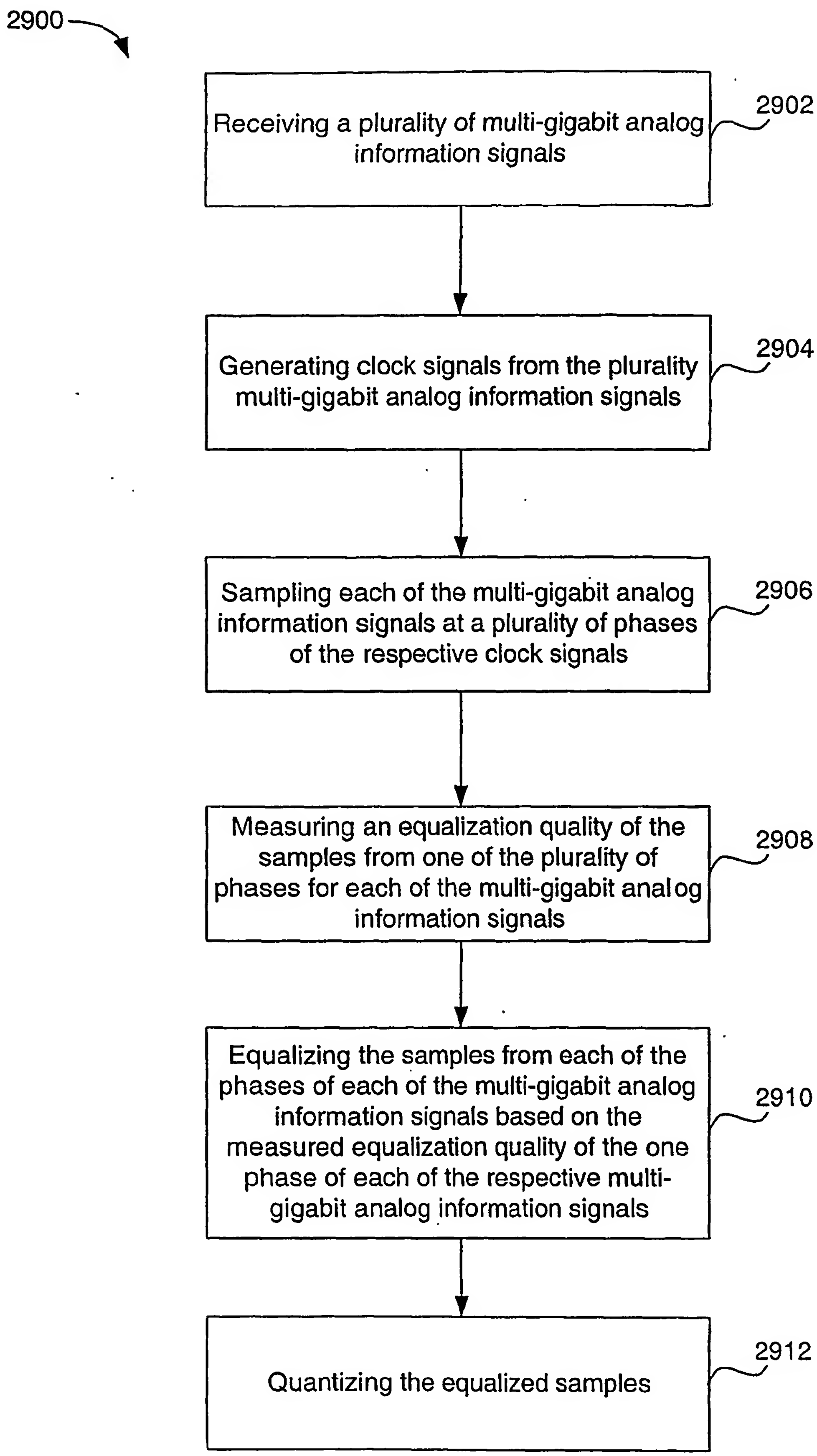

2900
Receiving a plurality of multi-gigabit analog information signals
2902
Generating clock signals from the plurality multi-gigabit analog information signals
2904
Sampling each of the multi-gigabit analog information signals at a plurality of phases of the respective clock signals
2906
Measuring an equalization quality of the samples from one of the plurality of phases for each of the multi-gigabit analog information signals
2908
Equalizing the samples from each of the phases of each of the multi-gigabit analog information signals based on the measured equalization quality of the one phase of each of the respective multi-gigabit analog information signals
2910
Quantizing the equalized samples
2912

FIG. 29

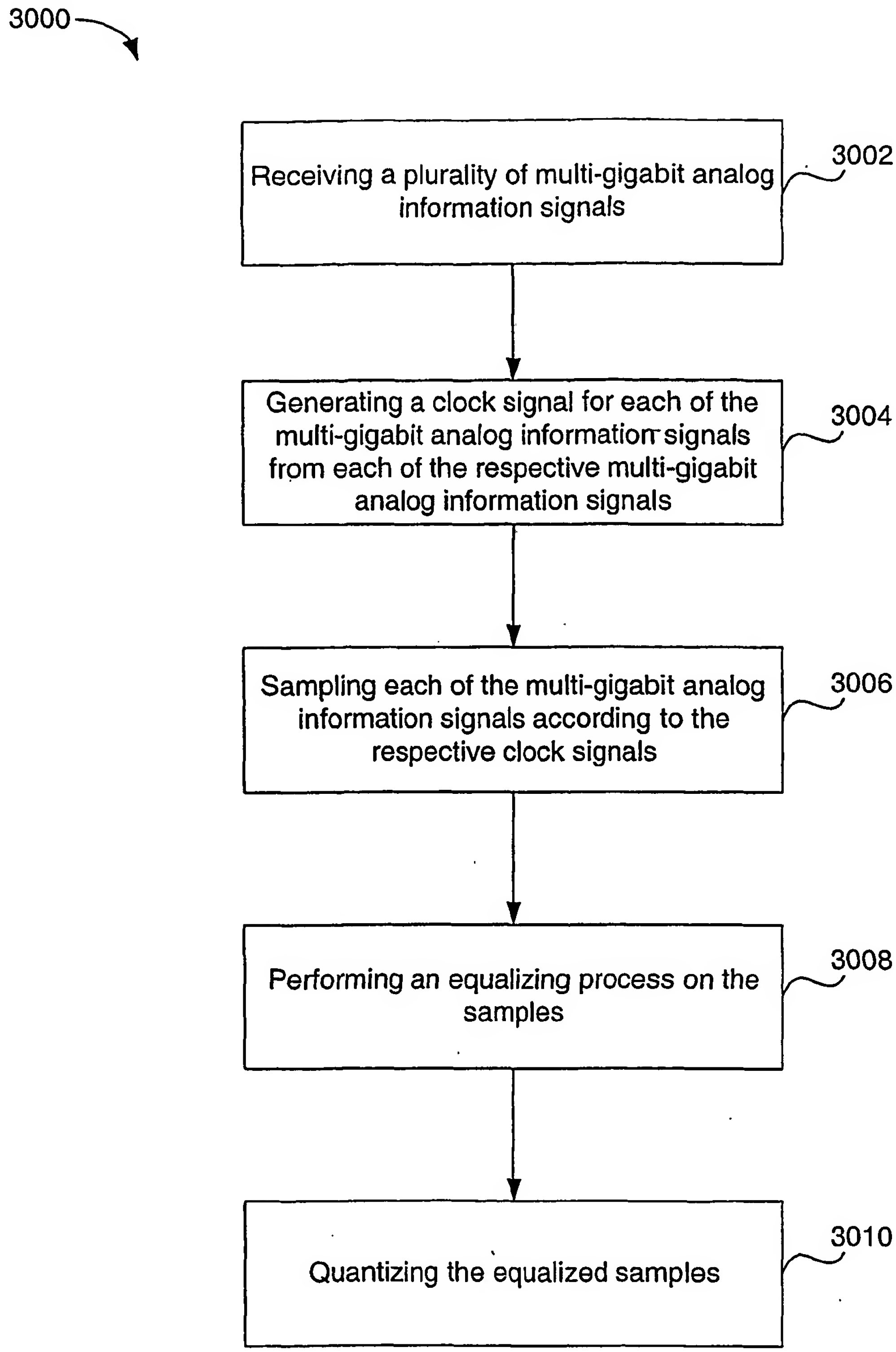

3000
Receiving a plurality of multi-gigabit analog information signals
3002
Generating a clock signal for each of the multi-gigabit analog information signals from each of the respective multi-gigabit analog information signals
3004
Sampling each of the multi-gigabit analog information signals according to the respective clock signals
3006
Performing an equalizing process on the samples
3008
Quantizing the equalized samples
3010

FIG. 30

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8 November 2001 (08.11.2001)

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(72) Inventors: BUCHWALD, Aaron, W.; 38 Via Rubino, Newport Coast, CA 92657 (US). JIANG, Xicheng; 1 Silent Night, Irving, CA 92612 (US). WANG, Hui; 242 Sonoma Aisle, Irvine, CA 92618 (US). BAUMER, Howard, A.; 26041 El Prado, Laguna Hills, CA 92653 (US). MADISETTI, Avanindra; 5 Willow View Lane, Coto De Caza, CA 92679 (US).

(74) Agents: SOKOHL, Robert, E. et al.; Sterne, Kessler, Goldstein & Fox P.L.L.C., Suite 600, 1100 New York Avenue, N.W., Washington, DC 20005-3934 (US).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EE, ES FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

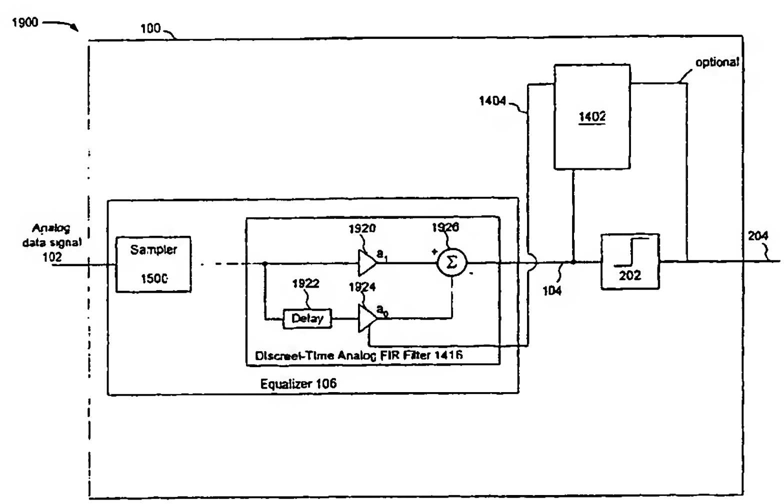
(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

(88) Date of publication of the international search report: 23 May 2002

[Continued on next page]

(54) Title: METHODS AND SYSTEMS FOR ADAPTIVE RECEIVER EQUALIZATION



(57) Abstract: Methods and systems for minimizing distortions in an analog data signal include equalizing the analog data signal at a receive end. In an embodiment, the invention adapts equalization parameters to a signal path associated with the analog data signal. Adaptive control logic is implemented with analog and/or digital components. In an embodiment, the invention equalizes a discreet-time analog representation of an analog data signal. In an embodiment, the invention digitally controls equalization parameters. In an embodiment, a resultant equalized analog data signal is digitized. In an example implementation, an analog data signal is sampled, a quality of the samples is measured, and one or more equalization parameters are adjusted with digital controls as needed to minimize distortion of the samples. The equalized samples are then digitized. The present invention is suitable for lower rate analog data signals and multi-gigabit data rate analog signals.

WO 01/84724 A3

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 01/13613

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04L25/03

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ, INSPEC, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 650 954 A (MINUHIN VADIM BORIS) 22 July 1997 (1997-07-22)	1,2,11, 12, 15-19,21
A	column 1, line 56 -column 2, line 50 column 2, line 57 -column 3, line 15 column 12, line 60 -column 13, line 15 figure 4 ---	3,4
X	US 5 966 415 A (BLISS WILLIAM G ET AL) 12 October 1999 (1999-10-12) abstract column 4, line 40 - line 65 column 7, line 25 -column 8, line 5 column 13, line 7 - line 37 ---	1-3,11, 12,16, 17,21
	-/--	

[X] Further documents are listed in the continuation of box C.

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Date of the actual completion of the international search	Date of mailing of the international search report
17 January 2002	24/01/2002

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Litton, R

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 01/13613

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	EP 0 805 447 A (CIRRUS LOGIC INC) 5 November 1997 (1997-11-05) page 5, line 25 - line 34 page 13, line 6 - line 32 ---	1,2,11, 12,16,21 3,4
A	EP 0 483 439 A (IBM) 6 May 1992 (1992-05-06) page 2, line 12 - line 45 ---	1-4,11, 12,16,21
A	US 5 881 108 A (WERNER JEAN-JACQUES ET AL) 9 March 1999 (1999-03-09) abstract page 10, line 35 - line 55 -----	1,11-13, 16,21

6

INTERNATIONAL SEARCH REPORT

ɹrmation on patent family members

Intern˘ ıal Application No
PCT/US 01/13613

Patent document cited in search report		Publication date	Patent family member(s)			Publication date
US 5650954	A	22-07-1997	US	5854717	A	29-12-1998
US 5966415	A	12-10-1999	NONE			
EP 0805447	A	05-11-1997	EP	0805447	A2	05-11-1997
			JP	10092119	A	10-04-1998
EP 0483439	A	06-05-1992	EP	0483439	A1	06-05-1992
			DE	69020568	D1	03-08-1995
			JP	2055595	C	23-05-1996
			JP	4227129	A	17-08-1992
			JP	7093594	B	09-10-1995
			US	5319674	A	07-06-1994
US 5881108	A	09-03-1999	NONE			